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The TTL Data Book

Volume 1

1984

Indexes, Product Guide
General Information

TEXAS
INSTRUMENTS

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Volume 1

TEXAS
INSTRUMENTS

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INTRODUCTION

Texas Instruments presents important technical information on the industry's broadest and most advanced families of TTL integrated circuits in the TTL data books, volumes 1 through 4.

The TTL Data Book—Volume 1 includes Alphanumeric and Functional Indexes to all bipolar digital devices available or under development, showing the current technologies for each type. Logic symbols prepared in anticipation of IEEE Std. 91-1982 and pin assignments for all bipolar devices are shown in the Product Guide section, together with typical performance data and chip carrier information. Package dimensions are given in the Mechanical Data section.

The TTL Data Book—Volume 2 comprehends complete specifications on five series of Transistor-Transistor-Logic circuits: Standard TTL Circuits (Series 54/74), High-Speed TTL Circuits (Series 54H/74H), Low-Power TTL Circuits (Series 54L), Low-Power Schottky[†] TTL Circuits (Series 54LS/74LS), and Schottky TTL Circuits (Series 54S/74S).

The TTL Data Book—Volume 3 contains complete specifications on the most advanced Families of TTL integrated circuits: Advanced Low-Power Schottky[†] (Series 54ALS/74ALS) and Advanced Schottky (Series54AS/74AS), with circuits capable of twice the data throughput compared to Low-Power Schottky TTL (54LS/74LS) and Schottky TTL (54S/74S) devices.

The TTL Data Book—Volume 4 describes a series of high-complexity bipolar digital building blocks and support functions designed specifically for implementing high-performance Computer or Controller systems. Included are specifications for high-performance Schottky[†] TTL memories (RAMs, ROMs, PROMs, and FIFOs) and for Field-Programmable Logic devices.

The TTL data books, volumes 1 through 4, will be a meaningful addition to your technical library. They replace all previous versions of:

- *The TTL Data Book*
- *The ALS/AS Logic Circuits Data Book*
- *The Bipolar Microprocessor Components Data Book.*

[†] Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

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SN54LS373	SN74LS373	2
SN54S373	SN74S373	2
SN54ALS374	SN74ALS374	3
SN54AS374	SN74AS374	3
SN54LS374	SN74LS374	2
SN54S374	SN74S374	2
SN54LS375	SN74LS375	2
SN54376	SN74376	2
SN54LS377	SN74LS377	2
SN54LS378	SN74LS378	2
SN54LS379	SN74LS379	2
SN54LS381	SN74LS381	2
SN54S381	SN74S381	2
SN54LS382	SN74LS382	2
SN54LS384	SN74LS384	2
SN54LS385	SN74LS385	2
SN54LS386	SN74LS386	2
SN54390	SN74390	2
SN54LS390	SN74LS390	2
SN54393	SN74393	2
SN54LS393	SN74LS393	2
SN54AS395	SN74AS395	3
SN54LS395A	SN74LS395A	2
SN54LS396	SN74LS396	2
SN54LS398	SN74LS398	2
SN54LS399	SN74LS399	2
SN54S412	SN74S412	2

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Device Types		Volume
SN54LS422	SN74LS422	2
SN54LS423	SN74LS423	2
SN54425	SN74425	2
SN54426	SN74426	2
	SN74S428	4
SN54S436	SN74S436	2
SN54S437	SN74S437	2
SN54LS440	SN74LS440	2
SN54LS441	SN74LS441	2
SN54LS442	SN74LS442	2
SN54LS443	SN74LS443	2
SN54LS444	SN74LS444	2
SN54LS445	SN74LS445	2
SN54LS446	SN74LS446	2
SN54LS447	SN74LS447	2
SN54LS448	SN74LS448	2
SN54LS449	SN74LS449	2
SN54ALS465A	SN74ALS465A	3
SN54LS465	SN74LS465	2
SN54ALS466A	SN74ALS466A	3
SN54LS466	SN74LS466	2
SN54ALS467A	SN74ALS467A	3
SN54LS467	SN74LS467	2
SN54ALS468A	SN74ALS468A	3
SN54LS468	SN74LS468	2
	SN74LS481	4
	SN74S481	4
SN54S482	SN74S482	4
SN54S484A	SN74S484A	4
SN54S485A	SN74S485A	4
SN54490	SN74490	2
SN54LS490	SN74LS490	2
SN54ALS518	SN74ALS518	3
SN54ALS519	SN74ALS519	3
SN54ALS520	SN74ALS520	3
SN54ALS521	SN74ALS521	3
SN54ALS522	SN74ALS522	3
SN54ALS526	SN74ALS526	3
SN54ALS527	SN74ALS527	3
SN54ALS528	SN74ALS528	3
SN54ALS533	SN74ALS533	3
SN54AS533	SN74AS533	3
SN54ALS534	SN74ALS534	3
SN54AS534	SN74AS534	3
SN54ALS538	SN74ALS538	3
SN54ALS539	SN74ALS539	3
SN54ALS540	SN74ALS540	3
SN54LS540	SN74LS540	2
SN54ALS541	SN74ALS541	3
SN54LS541	SN74LS541	2
SN54ALS560A	SN74ALS560A	3
SN54ALS561A	SN74ALS561A	3
SN54ALS563	SN74ALS563	3
SN54ALS564	SN74ALS564	3
SN54ALS568A	SN74ALS568A	3
SN54ALS569A	SN74ALS569A	3
SN54ALS573	SN74ALS573	3
SN54AS573	SN74AS573	3
SN54ALS574	SN74ALS574	3
SN54AS574	SN74AS574	3
SN54ALS575	SN74ALS575	3
SN54AS575	SN74AS575	3

Device Types		Volume
SN54ALS576	SN74ALS576	3
SN54AS576	SN74AS576	3
SN54ALS577	SN74ALS577	3
SN54AS577	SN74AS577	3
SN54ALS580	SN74ALS580	3
SN54AS580	SN74AS580	3
SN54LS589	SN74LS589	2
SN54LS590	SN74LS590	2
SN54LS591	SN74LS591	2
SN54LS592	SN74LS592	2
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SN54LS596	SN74LS596	2
SN54LS597	SN74LS597	2
SN54LS598	SN74LS598	2
SN54LS599	SN74LS599	2
	SN74LS600A	2
	SN74LS601A	2
	SN74LS602A	2
	SN74LS603A	2
SN54LS604	SN74LS604	2
SN54LS605	SN74LS605	2
SN54LS606	SN74LS606	2
SN54LS607	SN74LS607	2
SN54LS608	SN74LS608	2
SN54LS610	SN74LS610	2
SN54LS611	SN74LS611	2
SN54LS612	SN74LS612	2
SN54LS613	SN74LS613	2
SN54LS618	SN74LS618	2
SN54LS619	SN74LS619	2
SN54ALS620A	SN74ALS620A	3
SN54AS620	SN74AS620	3
SN54LS620	SN74LS620	2
SN54ALS621A	SN74ALS621A	3
SN54AS621	SN74AS621	3
SN54LS621	SN74LS621	2
SN54ALS622A	SN74ALS622A	3
SN54AS622	SN74AS622	3
SN54LS622	SN74LS622	2
SN54ALS623A	SN74ALS623A	3
SN54AS623	SN74AS623	3
SN54LS623	SN74LS623	2
SN54LS624	SN74LS624	2
SN54LS625	SN74LS625	2
SN54LS626	SN74LS626	2
SN54LS627	SN74LS627	2
SN54LS628	SN74LS628	2
SN54LS629	SN74LS629	2
SN54LS630	SN74LS630	2
SN54LS631	SN74LS631	2
SN54ALS632	SN74ALS632	3
SN54ALS633	SN74ALS633	3
SN54ALS634	SN74ALS634	3
SN54ALS635	SN74ALS635	3
SN54LS636	SN74LS636	2
SN54LS637	SN74LS637	2
SN54ALS638A	SN74ALS638A	3
SN54AS638	SN74AS638	3
SN54LS638	SN74LS638	2
SN54ALS639A	SN74ALS639A	3

Device Types		Volume
SN54AS639	SN74AS639	3
SN54LS639	SN74LS639	2
SN54ALS640A	SN74ALS640A	3
SN54AS640	SN74AS640	3
SN54LS640	SN74LS640	2
SN54ALS641A	SN74ALS641A	3
SN54AS641	SN74AS641	3
SN54LS641	SN74LS641	2
SN54ALS642A	SN74ALS642A	3
SN54AS642	SN74AS642	3
SN54LS642	SN74LS642	2
SN54ALS643A	SN74ALS643A	3
SN54AS643	SN74AS643	3
SN54LS643	SN74LS643	2
SN54ALS644A	SN74ALS644A	3
SN54AS644	SN74AS644	3
SN54LS644	SN74LS644	2
SN54ALS645A	SN74ALS645A	3
SN54AS645	SN74AS645	3
SN54LS645	SN74LS645	2
SN54ALS646	SN74ALS646	3
SN54AS646	SN74AS646	3
SN54LS646	SN74LS646	2
SN54ALS647	SN74ALS647	3
SN54LS647	SN74LS647	2
SN54ALS648	SN74ALS648	3
SN54AS648	SN74AS648	3
SN54LS648	SN74LS648	2
SN54ALS649	SN74ALS649	3
SN54LS649	SN74LS649	2
SN54ALS651	SN74ALS651	3
SN54AS651	SN74AS651	3
SN54LS651	SN74LS651	2
SN54ALS652	SN74ALS652	3
SN54AS652	SN74AS652	3
SN54LS652	SN74LS652	2
SN54ALS653	SN74ALS653	3
SN54LS653	SN74LS653	2
SN54ALS654	SN74ALS654	3
SN54LS654	SN74LS654	2
SN54LS668	SN74LS668	2
SN54LS669	SN74LS669	2
SN54LS670	SN74LS670	2
SN54LS671	SN74LS671	2
SN54LS672	SN74LS672	2
SN54LS673	SN74LS673	2
SN54LS674	SN74LS674	2
SN54ALS677	SN74ALS677	3
SN54ALS678	SN74ALS678	3
SN54ALS679	SN74ALS679	3
SN54ALS680	SN74ALS680	3
SN54LS681	SN74LS681	2
SN54LS682	SN74LS682	2
SN54LS683	SN74LS683	2
SN54LS684	SN74LS684	2
SN54LS685	SN74LS685	2
SN54LS686	SN74LS686	2
SN54LS687	SN74LS687	2
SN54ALS688	SN74ALS688	3
SN54LS688	SN74LS688	2
SN54ALS689	SN74ALS689	3
SN54LS689	SN74LS689	2

Device Types		Volume
SN54LS690	SN74LS690	2
SN54LS691	SN74LS691	2
SN54LS692	SN74LS692	2
SN54LS693	SN74LS693	2
SN54LS696	SN74LS696	2
SN54LS697	SN74LS697	2
SN54LS698	SN74LS698	2
SN54LS699	SN74LS699	2
SN54AS756	SN74AS756	3
SN54AS757	SN74AS756	3
SN54AS758	SN74AS758	3
SN54AS759	SN74AS759	3
SN54AS760	SN74AS760	3
SN54AS762	SN74AS762	3
SN54AS763	SN74AS763	3
SN54AS800	SN74AS800	3
SN54AS802	SN74AS802	3
SN54ALS804	SN74ALS804	3
SN54AS804A	SN74AS804A	3
SN54ALS805	SN74ALS805	3
SN54AS805A	SN74AS805A	3
SN54ALS808	SN74ALS808	3
SN54AS808A	SN74AS808A	3
SN54AS821	SN74AS821	3
SN54AS822	SN74AS822	3
SN54AS823	SN74AS823	3
SN54AS824	SN74AS824	3
SN54AS825	SN74AS825	3
SN54AS826	SN74AS826	3
SN54ALS832	SN74ALS832	3
SN54AS832A	SN74AS832A	3
SN54ALS841	SN74ALS841	3
SN54AS841	SN74AS841	3
SN54ALS842	SN74ALS842	3
SN54AS842	SN74AS842	3
SN54ALS843	SN74ALS843	3
SN54AS843	SN74AS843	3
SN54ALS844	SN74ALS844	3
SN54AS844	SN74AS844	3
SN54ALS845	SN74ALS845	3
SN54AS845	SN74AS845	3
SN54ALS846	SN74ALS846	3
SN54AS846	SN74AS846	3
SN54AS850	SN74AS850	3
SN54AS851	SN74AS851	3
SN54AS852	SN74AS852	3
SN54AS856	SN74AS856	3
SN54ALS857	SN74ALS857	3
SN54AS857	SN74AS857	3
SN54AS866	SN74AS866	3
SN54AS867	SN74AS867	3
SN54AS869	SN74AS869	3
SN54AS870	SN74AS870	3
SN54AS871	SN74AS871	3
SN54ALS873	SN74ALS873	3
SN54AS873	SN74AS873	3
SN54ALS874	SN74ALS874	3
SN54AS874	SN74AS874	3
SN54ALS876	SN74ALS876	3
SN54AS876	SN74AS876	3
SN54AS877	SN74AS877	3
SN54ALS878	SN74ALS878	3

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Device Types		Volume
SN54AS878	SN74AS878	3
SN54ALS879	SN74ALS879	3
SN54AS879	SN74AS879	3
SN54ALS880	SN74ALS880	3
SN54AS880	SN74AS880	3
SN54AS881A	SN74AS881A	3
SN54AS882	SN74AS882	3
SN54AS885	SN74AS885	3
SN54AS888	SN74AS888	4
SN54AS889	SN74AS889	4
SN54AS890	SN74AS890	4
SN54AS891	SN74AS891	4
SN54AS897	SN74AS897	4
SN54ALS1000A	SN74ALS1000A	3
SN54AS1000	SN74AS1000	3
SN54ALS1002A	SN74ALS1002A	3
SN54ALS1003A	SN54ALS1003A	3
SN54ALS1004	SN54ALS1004	3
SN54AS1004	SN74AS1004	3
SN54ALS1005	SN74ALS1005	3
SN54ALS1008A	SN74ALS1008A	3
SN54AS1008	SN74AS1008	3
SN54ALS1010A	SN74ALS1010A	3
SN54ALS1011A	SN74ALS1011A	3
SN54ALS1020A	SN74ALS1020A	3
SN54ALS1032A	SN74ALS1032A	3
SN54AS1032	SN74AS1032	3
SN54ALS1034	SN74ALS1034	3
SN54AS1034	SN74AS1034	3
SN54ALS1035	SN74ALS1035	3
SN54AS1036	SN74AS1036	3
SN54ALS1240	SN74ALS1240	3
SN54ALS1241	SN74ALS1241	3
SN54ALS1242	SN74ALS1242	3
SN54ALS1243	SN74ALS1243	3
SN54ALS1244A	SN74ALS1244A	3
SN54ALS1245	SN74ALS1245	3
SN54ALS1616	SN74ALS1616	4
SN54ALS1620	SN74ALS1620	3
SN54ALS1621	SN74ALS1621	3
SN54ALS1622	SN74ALS1622	3
SN54ALS1623	SN74ALS1623	3
SN54ALS1638	SN74ALS1638	3
SN54ALS1639	SN74ALS1639	3
SN54ALS1640A	SN74ALS1640A	3
SN54ALS1641	SN74ALS1641	3
SN54ALS1642	SN74ALS1642	3
SN54ALS1643	SN74ALS1643	3
SN54ALS1644	SN74ALS1644	3
SN54ALS1645A	SN74ALS1645A	3
SN54AS2620	SN74AS2620	3
SN54AS2623	SN74AS2623	3
SN54AS2640	SN74AS2640	3
SN54AS2645	SN74AS2645	3
SN54ALS8003	SN74ALS8003	3

Device Types		Volume
SN54PAL16L8A	SN74PAL16L8A	4
SN54PAL16R4A	SN74PAL16R4A	4
SN54PAL16R6A	SN74PAL16R6A	4
SN54PAL16R8A	SN74PAL16R8A	4
SN54PAL20L8A	SN74PAL20L8A	4
SN54PAL20R4A	SN74PAL20R4A	4
SN54PAL20R6A	SN74PAL20R6A	4
SN54PAL20R8A	SN74PAL20R8A	4
SN54PALR19L8	SN74PALR19L8	4
SN54PALR19R4	SN74PALR19R4	4
SN54PALR19R6	SN74PALR19R6	4
SN54PALR19R8	SN74PALR19R8	4
SN54PALT19L8	SN74PALT19L8	4
SN54PALT19R4	SN74PALT19R4	4
SN54PALT19R6	SN74PALT19R6	4
SN54PALT19R8	SN74PALT19R8	4
SN54PL839	SN74PL839	4
SN54PL840	SN74PL840	4
SBP9901		4
SBP9965		4
SBP9966		4
SBP9989		4
TBP18S030		4
TBP18SA030		4
TBP24S10		4
TBP24SA10		4
TBP24S41		4
TBP24SA41		4
TBP24S81		4
TBP24SA81		4
TBP28L22		4
TBP28LA22		4
TBP28L42		4
TBP28S42		4
TBP28SA42		4
TBP28L45		4
TBP28S45		4
TBP28L46		4
TBP28S46		4
TBP28SA46		4
TBP28L85A		4
TBP28S85A		4
TBP28L86A		4
TBP28S86A		4
TBP28SA86A		4
TBP28L165		4
TBP28S165		4
TBP28L166		4
TBP28S166		4

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

JANUARY 1984

description

Texas Instruments transistor-transistor-logic (TTL) family of high-performance bipolar digital integrated circuits comprises seven distinct series of compatible product lines. These product lines offer the digital systems designer a full spectrum of performance ranges in order to optimize system cost and performance. The available choices range from the very high performance of the Advanced Schottky-clamped[†] functions for systems operating typically up to 175 megahertz to low-power functions with power consumption of only one milliwatt per gate.

Typical characteristics of the seven TTL series offered are shown in Table I and their respective speed/power relationships are illustrated in Figure A.

SPEED-POWER RELATIONSHIPS OF DIGITAL IC FAMILIES‡

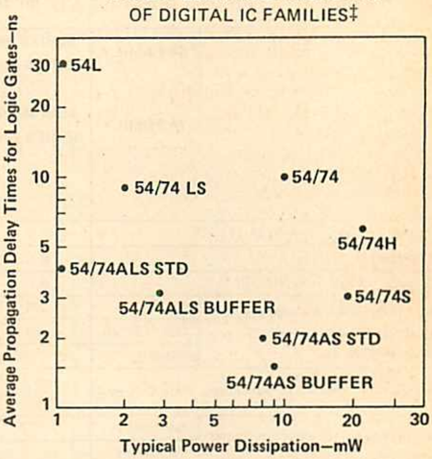

FIGURE A

‡ Typical saturated logic gate from the indicated families.

TABLE I—54/74 FAMILY TYPICAL SSI PERFORMANCE CHARACTERISTICS

SERIES		GATES		FLIP-FLOPS
	Speed-Power Product	Propagation Delay Time	Power Dissipation	Clock Input Frequency Range
54/74	100 pJ	10 ns	10 mW	dc to 35 MHz
54ALS/74ALS	4 pJ	4 ns	1 mW	dc to 50 MHz
54AS/74AS	15 pJ	1.5 ns	10 mW	dc to 175 MHz
54H/74H	132 pJ	6 ns	22 mW	dc to 50 MHz
54L	33 pJ	33 ns	1 mW	dc to 3 MHz
54LS/74LS	19 pJ	9.5 ns	2 mW	dc to 45 MHz
54S/74S	57 pJ	3 ns	19 mW	dc to 125 MHz

features

EASE OF SYSTEM DESIGN

- Full compatibility provides choice from seven distinct performance ranges
- Broad range of functions are offered in each series
- Diode-clamped inputs are provided on all high-performance functions
- Terminated,controlled-impedance lines are not normally required with TTL
- Low output impedance:
  Provides low a-c noise susceptibility
  Drives high-capacity loads

FULL COMPATIBILITY IS DESIGNED INTO TI TTL

- All series are designed for single 5-volt power supply
- All series provide one-volt or greater typical d-c noise margins
- Power dissipation relatively insensitive to operating frequency
- Switching times are guaranteed at full d-c loading
- Compatible with most logic families such as MOS, CMOS

[†] Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	54 FAMILY	SERIES 54 SERIES 54H	SERIES 54L	SERIES 54ALS SERIES 54AS SERIES 54LS	SERIES 54LS	SERIES 54S	UNIT
	74 FAMILY	SERIES 74 SERIES 74H		SERIES 74ALS SERIES 74AS SERIES 74LS WITH DIODE AND PNP INPUTS	SERIES 74LS WITH EMITTER INPUTS	SERIES 74S	
Supply voltage, V_{CC} (see Note 1)		7	8	7	7	7	V
Input voltage		5.5	5.5	7	5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5		5.5	5.5	V
Off-state (high-level) voltage applied to open-collector outputs of SSI circuits (see Note 3)	'06, '07	30					V
	'16, '17, '26	15					
	Others		8	7	7	7	
High-level voltage applied to a disabled 3-state output		5.5		5.5	5.5	5.5	V
Operating free-air temperature range	54 Family	−55 to 125					°C
	74 Family	0 to 70					
Storage temperature range		−65 to 150					°C

NOTES: 1. Voltage values, unless otherwise noted, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies between inputs that go directly into the same AND or NAND gate in the functional block diagram.

3. Ratings for MSI parts are given on the individual date sheets.

unused inputs of positive-AND/NAND gates

For optimum switching times and minimum noise susceptibility, unused inputs of AND or NAND gates should be maintained at a voltage greater than V_{OH} min (see tables of electrical characteristics), but not to exceed the absolute maximum rating. This eliminates the distributed capacitance associated with the floating input, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling unused inputs are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between V_{OH} min and 4.5 V. Series 54LS/74LS devices with diode inputs may be connected directly to V_{CC}.

b. Connect unused inputs to a used input if maximum drive capability of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.

c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient that exceeds the input maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor. Series 54LS/74LS devices with diode inputs may be connected directly to V_{CC}.

d. Connect unused inputs to any fixed-high-level compatible output such as the output of an inverter or NAND gate that has its input(s) grounded. Maximum high-level drive capability of the output should not be exceeded.

input-current requirements

Input-current requirements reflect worst-case conditions over the specified recommended operating free-air temperature and V_{CC} ranges. The table below shows maximum input current requirements and nominal base resistor values for standard loads in each TTL series. A standard load is defined as an input connected to a single emitter or diode that is associated with a pull-up resistor having the value indicated in the table. However, some inputs are tied to more than one input transistor (or diode), or the base-resistor values of some inputs have been changed either to reduce input-current requirements or to improve performance. Therefore, the input-current requirements may vary. Consult the electrical characteristics table for the particular device type to determine the input-current requirements of each input.

STANDARD INPUTS (ONE LOAD)[†]

SERIES	NOMINAL VALUE OF INPUT PULL-UP RESISTOR	MAXIMUM HIGH-LEVEL INPUT CURRENT	MAXIMUM LOW-LEVEL INPUT CURRENT
54/74	4 kΩ	40 μA	−1.6 mA
54ALS/74ALS	40 kΩ	20 μA	−0.1 mA
54AS/74AS	8 kΩ	20 μA	−0.5 mA
54H/74H	2.8 kΩ	50 μA	−2 mA
54L[‡]	40 kΩ	10 μA	−0.18 mA
	8 kΩ	20 μA	−0.8 mA
54LS/74LS[‡]	18 kΩ	20 μA	−0.4 mA
	12 kΩ	20 μA	−0.2 mA
54S/74S	2.8 kΩ	50 μA	−2 mA

[‡] Series 54L and 54LS/74LS have two different types of inputs as shown.

Since low-level input current is primarily a function of the input base resistor, two or more inputs of the same NAND or AND gate may be tied together and still be considered one load at a low logic level, but at a high logic level, each *input is* an additional load.

Currents into input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

drive capability

TYPICAL FAN-OUT[†]

OUTPUT DEVICE		LOAD DEVICE					
		SN74 SN54	SN74ALS SN54ALS	SN74AS SN54AS	SN74H SN54H	SN74LS SN54LS	SN74S SN54S
SN74/SN54	Standard	10	80	80	8	40	8
	Buffer	30	240	240	24	120	24
SN74ALS/SN54ALS	Standard	5	40	40	4	20	4
	Buffer	15	120	120	12	60	12
SN74AS/SN54AS	Standard	12	100	100	10	50	10
	Buffer	30	240	240	24	120	24
SN74H/SN54H	Standard	12	100	100	10	50	10
	Buffer	37	300	300	30	150	30
SN74LS/SN54LS	Standard	5	40	40	4	20	4
	Buffer	15	120	120	12	60	12
SN74S/SN54S	Standard	12	100	100	10	50	10
	Buffer	37	300	300	30	150	30

[†] The tables on this page provide an overview of the performance of TI's digital logic families. The electrical characteristics of specific devices within each family may vary. Please consult the appropriate TI data sheet or data book for complete specifications.

GLOSSARY
TTL SYMBOLS, TERMS, AND DEFINITIONS

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

PART I — OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

f_{max}	**Maximum clock frequency** The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.
I_{CC}	**Supply current** The current into* the V_{CC} supply terminal of an integrated circuit.
I_{CCH}	**Supply current, outputs high** The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level.
I_{CCL}	**Supply current, outputs low** The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level.
I_{IH}	**High-level input current** The current into* an input when a high-level voltage is applied to that input.
I_{IL}	**Low-level input current** The current into* an input when a low-level voltage is applied to that input.
I_{OH}	**High-level output current** The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.
I_{OL}	**Low-level output current** The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.
I_{OS}	**Short-circuit output current** The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).
I_{OZH}	**Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied** The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output. NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

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*Current out of a terminal is given as a negative value.

I_{OZL}	**Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied** The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output. NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.
V_{IH}	**High-level input voltage** An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.
V_{IK}	**Input clamp voltage** An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.
V_{IL}	**Low-level input voltage** An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.
V_{OH}	**High-level output voltage** The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.
V_{OL}	**Low-level output voltage** The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.
t_a	**Access time** The time interval between the application of a specific input pulse and the availability of valid signals at an output.
t_{dis}	**Disable time (of a three-state output)** The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. ($t_{dis} = t_{PHZ}$ or t_{PLZ}).
t_{en}	**Enable time (of a three-state output)** The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). ($t_{en} = t_{PZH}$ or t_{PZL}).

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*Current out of a terminal is given as a negative value.

t_h	**Hold time** The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal. NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed. 2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.
t_{pd}	**Propagation delay time** The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (t_{pd} = t_{PHL} or t_{PLH}).
t_{PHL}	**Propagation delay time, high-to-low-level output** The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.
t_{PHZ}	**Disable time (of a three-state output) from high level** The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.
t_{PLH}	**Propagation delay time, low-to-high-level output** The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.
t_{PLZ}	**Disable time (of a three-state output) from low level** The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.
t_{PZH}	**Enable time (of a three-state output) to high level** The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.
t_{PZL}	**Enable time (of a three-state output) to low level** The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.
t_{sr}	**Sense recovery time** The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.
t_{su}	**Setup time** The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal. NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed. 2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.
t_w	**Pulse duration (width)** The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

PART II — CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate Equivalent Circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

Large-Scale Integration, LSI

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

Medium-Scale Integration, MSI

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

Small-Scale Integration, SSI

Integrated circuits of less complexity than medium-scale integration (MSI).

Very-Large-Scale Integration, VLSI

The description of any IC technology that is much more complex than large-scale integration (LSI), and involves a much higher equivalent gate count. At this time an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
→ = value/level or resulting value/level is routed to indicated destination
↶ = value/level is re-entered
X = irrelevant (any input, including transitions)
Z = off (high-impedance) state of a 3-state-output
a . . h = the level of steady-state inputs at inputs A through H respectively
Q_0 = level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$ = complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n = level of Q before the most recent active transition indicated by ↓ or ↑
⎍ = one high-level pulse
⊔ = one low-level pulse
TOGGLE = each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⊔, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

EXPLANATION OF FUNCTION TABLES

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

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GATES AND INVERTERS

POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Hex 2-Input Gates	'804		●	A					3
Hex Inverters	'04	●			●	●	●	●	2
			A	●					3
	'1004		●	●					
Quadruple 2-Input Gates	'00	●			●	●	●	●	2
			A	●					3
	'1000		A	●					
Triple 3-Input Gates	'10	●			●	●	●	●	2
			●	●					3
	'1010		A						
Dual 4-Input Gates	'20	●			●	●	●	●	2
			A	●					3
	'1020		A						
8-Input Gates	'30	●			●	●	●	●	2
			●	●					3
13-Input Gates	'133							●	2
			●						3
Dual 2-Input Gates	'8003		●						

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Hex Inverters	'05	●			●		●	●	2
			A						3
	'1005		●						
Quadruple 2-Input Gates	'01	●			●		●		2
			●						3
	'03	●				●	●	●	2
			A						3
	'1003		A						
Triple 3-Input Gates	'12	●					●		2
			●						3
Dual 4-Input Gates	'22	●			●		●	●	2
			A						3

POSITIVE-AND GATES

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
Hex 2-Input Gates	'808		●	A				3
Quadruple 2-Input Gates	'08	●				●	●	2
			●	●				3
	'1008		A	●				
Triple 3-Input Gates	'11				●	●	●	2
			●	●				3
	'1011		●					
Dual 4-Input Gates	'21					●		2
			●	●				3
Triple 4-Input AND/NAND	'800			▲				

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
Quadruple 2-Input Gates	'09	●				●	●	2
			●					3
Triple 3-Input Gates	'15				●	●	●	2
			●					3

POSITIVE-OR GATES

DESCRIPTION	TYP	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Hex 2-Input Gates	'832		●	A			3
Quadruple 2-Input Gates	'32	●			●	●	2
			●	●			3
	'1032		A	●			
Triple 4-Input OR/NOR	'802			▲			

POSITIVE-NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	L	LS	S	
Hex 2-Input Gates	'805		●	A				3
Quadruple 2-Input Gates	'02	●			●	●	●	2
			●	●				3
	'1002		A					
Triple 3-Input Gates	'27	●				●		2
			●	●				3
Dual 4-Input Gates with Strobe	'25	●						2
Dual 5-Input Gates	'260						●	

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Hex Inverters	'14	●			●		2
	'19				●		
Octal Inverters	'619				●		
Dual 4-Input Positive-NAND	'13	●			●		
	'18				●		
Triple 4-Input Positive-NAND	'618				●		
Quadruple 2-Input Positive-NAND	'24				●		
	'132	●			●	●	

CURRENT-SENSING GATES

DESCRIPTION	TYPE	TECHNOLOGY			VOLUME
		ALS	AS	LS	
Hex	'63			●	2

DELAY ELEMENTS

DESCRIPTION	TYP	TECHNOLOGY			VOLUME
		ALS	AS	LS	
Inverting & Non-Inverting Elements, 2-INPUT NAND Buffers	'31			●	2

●Denotes available technology.
▲Denotes planned new products.
A Denotes "A" suffix version available in the technology indicated.

GATES, EXPANDERS, BUFFERS, DRIVERS, AND TRANSCEIVERS

AND-OR-INVERT GATES

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
2-Wide 4-Input	'55				●	●	●		2
4-Wide 4-2-3-2 Input	'64							●	
4-Wide 2-2-3-2 input	'54				●				
4-Wide 2-Input	'54	●							
4-Wide 2-3-3-2 input	'54					●	●		
Dual 2-Wide 2-Input	'51	●			●	●	●	●	

AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	S	
4-Wide 4-2-3-2-Input	'65				●	2

EXPANDABLE GATES

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	L	LS	
Dual 4-Input Positive-NOR With Strobe	'23	●						2
4-Wide AND-OR	'52				●			
4-Wide AND-OR-INVERT	'53	●			●			
2-Wide AND-OR-INVERT	'55				●	●	●	
Dual 2-Wide AND-OR-INVERT	'50	●			●			

EXPANDERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	H	
Dual 4-Input	'60	●			●	2
Triple 3-Input	'61				●	
3-2-2-3-Input AND-OR	'62				●	

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Hex	'07	●					2
	'17	●					
	'35		▲				3
	'1035		●				
Hex Inverter	'06	●					2
	'16	●					
	'1005		●				3
Quad 2-Input Positive-NAND	'26	●					2
	'38	●			●	●	
			A				3
	'39	●					2
	'1003		A				3
Quad 2-Input Positive-NOR	'33	●			●		2
			A				3

BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Non-inverting Octal Buffers/Drivers	'757			▲			3
	'760			▲			
Inverting Octal Buffers/Drivers	'756			▲			
	'763			▲			
Inverting and Non-Inverting Octal Buffers/Drivers	'762			▲			
Non-Inverting Quad Transceivers	'759			▲			
Inverting Quad Transceivers	'758			▲			

GATES, BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Non-Inverting Octal Buffers/Drivers	'241				●	●	2
			A	●			3
	'244				●	●	2
			A	●			3
	'465				●		2
			A				3
	'467				●		2
			A				3
	'541				●		2
			▲				3
	'1241¶		▲				
	'1244¶		A				
Inverting Octal Buffers/Drivers	'231			●			
	'240				●	●	2
			A	●			3
	'466				●		2
			A				3
	'468				●		2
			A				3
	'540				●		2
			▲				3
	'1240¶		●				
Inverting and Non-Inverting Octal Buffers/Drivers	'230			●			
Octal Transceivers	'245				●		2
			A	▲			3
	'1245		●				
Non-inverting Hex Buffers/Drivers	'365	A			A		2
			▲				3
	'367	A			A		2
			▲				3
Inverting Hex Buffers/Drivers	'366	A			A		2
			▲				3
	'368	A			A		2
			▲				3
Quad Buffers/Drivers with Independent Output Controls	'125	●			A		2
	'126	●			A		
	'425	●					
	'426	●					
Non-Inverting Quad Transceivers	'243				●		3
			A	●			
	'1243¶		▲				
Inverting Quad Transceivers	'242				●		2
			A	●			3
	'1242¶		▲				
Quad Transceivers with Storage	'226					●	2
12-Input NAND Gate	'134					●	
Controller and Bus Driver for 8080A System	'428					●	

50-OHM/75-OHM LINE DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	S	
Hex 2-Input Positive-NAND	'804		●	A		3
Hex 2-Input Positive-NOR	'805		●	A		
Hex 2-Input Positive-AND	'808		●	A		
Hex 2-Input Positive-OR	'832		●	A		
Quad 2-Input Positive-NOR	'128	●				2
Dual 4-Input Positive-NAND	'140				●	

● Denotes available tchnology.
▲ Denotes planned new products.
¶ Denotes very low power.
A Denotes "A" suffix version available in the technology indicated.

BUFFERS, DRIVERS, TRANSCEIVERS, AND CLOCK GENERATORS

BUFFERS, CLOCK/MEMORY DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	H	LS	S	VOLUME
Hex 2-Input Positive-NAND	'804		●	A				3
Hex 2-Input Positive-NOR	'805		●	A				
Hex 2-Input Positive-AND	'808		●	A				
Hex 2-Input Positive-OR	'832		●	A				
Hex Inverter	'1004		●	●				
Hex Buffer	'34		▲	●				
	'1034		●	●				
Quad 2-Input Positive-NAND	'37	●				●	●	2
			A					3
	'1000		A	●				
Quad 2-Input Positive-NOR	'28	●				●		2
			A					3
	'1002		A					
	'1036			●				
Quad 2-Input Positive-AND	'1008		A	●				
Quad 2-Input Positive-OR	'1032		A	●				
Triple 3-Input Positive-NAND	'1010		A					
Triple 3-Input Positive-AND	'1011		A					
Triple 4-Input AND-NAND	'800			▲				
Triple 4-Input OR-NOR	'802			▲				
Dual 4-Input Positive-NAND	'40	●			●	●	●	2
			A					3
	'1020		A					
Line Driver/Memory Driver with Series Damping Resistor	'436						●	2
Line Driver/Memory Driver	'437						●	

BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS AND DRIVERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY ALS	AS	LS	S	VOLUME
Quad with Bit Direction	3-State	'446			●		2
Controls	3-State	'449			●		
Quad Tridirection	OC	'440			●		
	OC	'441			●		
	3-State	'442			●		
	3-State	'443			●		
	3-State	'444			●		
	OC	'448			●		
4-Bit with Storage	3-State	'226				●	
Controller and Bus Driver for 8080A Systems		'428				●	4

OCTAL BUS TRANSCEIVERS/MOS DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	ALS	AS	LS	S	VOLUME
Inverting Outputs, 3-State	'2620			▲			3
	'2640			▲			
True Outputs, 3-State	'2623			▲			
	'2645			▲			

OCTAL BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS

DESCRIPTION		TYPE OF OUTPUT	TYPE	TECHNOLOGY ALS	AS	LS	VOLUME
12 mA/24 mA/48 mA/64 mA Sink, True Outputs	Low Power	3-State	'245	A	▲		3
						●	2
		OC	'621	A	●		3
						●	2
		3-State	'623	A	▲		3
						●	2
		OC, 3-State	'639	A	●		3
						●	2
		3-State	'652	▲	●		3
						●	2
		OC, 3-State	'654	▲			3
						●	2
	Very Low Power	OC	'1621	▲			3
		3-State	'1623	▲			
		OC, 3-State	'1639	▲			
12 mA/24 mA/48 mA/64 mA Sink, Inverting Outputs	Low Power	3-State	'620	A	●		
						●	2
		OC	'622	A	▲		3
						●	2
		OC, 3-State	'638	A	●		3
						●	2
		3-State	'651	▲	●		3
						●	2
		OC, 3-State	'653	▲			3
						●	2
	Very Low Power	3-State	'1620	▲			3
		OC	'1622	▲			
		OC, 3-State	'1638	▲			
12 mA/24 mA/48 mA/64 mA Sink, True Outputs	Low Power	OC	'641	A	●		
						●	2
		3-State	'645	A	●		3
						●	2
	Very Low Power	OC	'1641	▲			3
		3-State	'1645	A			
12 mA/24 mA/48 mA/64 mA Sink, Inverting Outputs	Low Power	3-State	'640	A	●		
						●	2
		OC	'642	A	●		3
						●	2
	Very Low Power	3-State	'1640	A			3
		OC	'1642	▲			
12 mA/24 mA/48 mA/64 mA Sink, True and Inverting Outputs	Low Power	3-State	'643	A	●		
						●	2
		OC	'644	A	●		3
						●	2
	Very Low Power	3-State	'1643	▲			3
		OC	'1644	▲			
Registered with Multiplex 12 mA/24 mA/48 mA/64 mA True Outputs		3-State	'646	▲	●		
						●	2
		OC	'647	▲			3
						●	2
Registered with Multiplexed 12 mA/24 mA/48 mA/64 mA Inverting Outputs		3-State	'648	▲	●		3
						●	2
		OC	'649	▲			3
						●	2
Universal Transceiver/ Port Controllers		3-State	'877		▲		3
			'852		▲		
			'856		▲		

●Denotes available technology.
▲Denotes planned new products.
A Denotes "A" suffix version available in the technology indicated.

FLIP-FLOPS

DUAL AND SINGLE FLIP-FLOPS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Dual J-K Edge-Triggered	'73						A		2
	'76						A		
	'78						A		
	'103				●				
	'106				●				
	'107						A		
	'108				●				
	'109	●					A		
			●	●					3
	'112						A	●	2
			A	▲					3
	'113						A	●	2
			A	▲					3
	'114						A	●	2
			A	▲					3
Single J-K Edge-Triggered	'70	●							2
	'101				●				
	'102				●				
Dual Pulse-Triggered	'73	●			●	●			
	'76	●			●				
	'78				●	●			
	'107	●							
Single Pulse-Triggered	'71				●	●			
	'72	●			●	●			
	'104	●							
	'105	●							
Dual J-K with Data Lockout	'111	●							
Single J-K with Data Lockout	'110	●							
Dual D-Type	'74	●			●	●	A	●	
			●	●					3

QUAD AND HEX FLIP-FLOPS

DESCRIPTION	NO. OF FFs	OUTPUTS	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
D Type	6	Q	'174	●			●	●	2
					●	●			3
			'378				●		2
	4	Q, $\overline{Q}$	'171				●		
			'175	●			●	●	
					●	●			3
			'379				●		2
J-K	4	Q	'276	●					
			'376	●					

OCTAL, 9-BIT, AND 10-BIT D-TYPE FLIP-FLOPS

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
True Data	Octal	3-State	'374		●	●			3
							●	●	2
		3-State	'574		●	●			3
True Data with Clear	Octal	2-State	'273		●				
				●			●		2
		3-State	'575		●	●			3
		3-State	'874		●	●			
		3-State	'878		●	●			
True with Enable	Octal	2-State	'377				●		2
Inverting	Octal	3-State	'534		●	●			3
		3-State	'564		●				
		3-State	'576		●	●			
Inverting with Clear	Octal	3-State	'577		●	●			
		3-State	'879		●	●			
Inverting with Preset	Octal	3-State	'876		●	●			
True	Octal	3-State	'825			▲			
Inverting	Octal	3-State	'826			▲			
True	9-Bit	3-State	'823			▲			
Inverting	9-Bit	3-State	'824			▲			
True	10-Bit	3-State	'821			●			
Inverting	10-Bit	3-State	'822			●			

●Denotes available tchnology.
▲Denotes planned new products.
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LATCHES AND MULTIVIBRATORS

QUAD LATCHES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	L	LS	
Dual 2-Bit Transparent	2-State	'75	●			●	●	2
	2-State	'77	●			●	●	
	2-State	'375					●	
S-R	2-State	'279	●				A	

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	L	
Single	'122	●			●	●	2
	'130	●					
	'422				●		
Dual	'123	●			●	●	
	'423				●		

OCTAL, 9-BIT, AND 10-BIT LATCHES

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
Transparent	Octal	3-State	'268					●	2
			'373				●	●	
					●	●			3
		3-State	'573		●	●			
Dual 4-Bit Transparent	Octal	2-State	'100	●					2
		2-State	'116	●					
		3-State	'873		●	●			
Inverting Transparent	Octal	3-State	'533		●	●			3
		3-State	'563		●				
		3-State	'580		●	●			
Dual 4-Bit Inverting Transparent	Octal	3-State	'880		●	●			
2-Input Multiplexed	Octal	3-State	'604				●		2
		OC	'605				●		
		3-State	'606				●		
		OC	'607				●		
Addressable	Octal	2-State	'259	●			●		
					▲				3
Multi-Mode Buffered	Octal	3-State	'412					●	2
True	Octal	3-State	'845		▲	▲			3
Inverting	Octal	3-State	'846		▲	▲			
True	9-Bit	3-State	'843		▲	▲			
Inverting	9-Bit	3-State	'844		▲	▲			
True	10-Bit	3-State	'841		▲	▲			
Inverting	10-Bit	3-State	'842		▲	▲			

MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Single	'121	●					2
Dual	'221	●			●		

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REGISTERS AND PROGRAMMABLE LOGIC ARRAYS

SHIFT REGISTERS

DESCRIPTION	NO. OF BITS	MODES				TYPE	TECHNOLOGY						VOLUME
		S-R	S-L	LOAD	HOLD		STD TTL	ALS	AS	L	LS	S	
Sign-Protected		X		X	X	'322					A		2
Parallel-In, Parallel-Out, Bidirectional	8	X	X	X	X	'198	●						
		X	X	X	X	'299					●	●	
								●	▲				3
		X	X	X	X	'323					●		2
								●	▲				3
	4	X	X	X	X	'194	●				A	●	2
									▲				3
Parallel-In, Parallel-Out, Registered Outputs	4	X	X	X	X	'671					●		2
		X	X	X	X	'672					●		
Parallel-In, Parallel-Out	8	X		X	X	'199	●						
	5	X		X		'96	●			●	●		
	4	X		X		'95	A			●	B		2
									▲				3
		X		X		'99				●			2
		X		X	X	'178	●						
		X		X	X	'179	●						
		X		X		'195	●				A	●	2
									▲				3
		X		X		'295					B		2
		X		X		'395					A		2
									▲				3
Serial-In Parallel-Out	16	X		X	X	'673					●		2
	8	X				'164	●			●	●		
								▲					3
Parallel-In, Serial-Out	16	X		X	X	'674					●		2
	8	X		X	X	'165	●				A		
								▲					3
		X		X	X	'166	●				A		2
								▲					3
Serial-In, Serial-Out	8	X				'91	A			●	●		2
	4	X		X		'94	●						

SHIFT REGISTERS WITH LATCHES

DESCRIPTION	NO. OF BITS	OUTPUTS	TYPE	TECHNOLOGY			VOLUME
				ALS	AS	LS	
Parallel-In, Parallel-Out with Output Latches	4	3-State	'671			●	2
		3-State	'672			●	
Serial-In, Parallel-Out with Output Latches	16	2-State	'673			●	
	8	Buffered	'594			●	
		3-State	'595			●	
		OC	'596			●	
		OC	'599			●	
Parallel-In, Serial-Out, with Input Latches	8	2-State	'597			●	
		3-State	'589			●	
Parallel I/O Ports with Input Latches, Multiplexed Serial Inputs	8	3-State	'598			●	

SIGN-PROTECTED REGISTERS

DESCRIPTION	NO. OF BITS	MODES				TYPE	TECHNOLOGY			VOLUME
		S-R	S-L	LOAD	HOLD		ALS	AS	LS	
Sign-Protected Register	8	X		X	X	'322			A	2

REGISTER FILES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY				VOLUME
			STD TTL	ALS	AS	LS	
8 Words × 2 Bits	3-State	'172	●				2
4 Words × 4 Bits	OC	'170	●			●	
	3-State	'670				●	
Dual 16 Words × 4 Bits	3-State	'870			▲		3
	3-State	'871			▲		

OTHER REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	L	LS	S	
Quadruple Multiplexers with Storage	'98				●			2
	'298	●				●		
	'398/9					●		
8-Bit Universal Shift Registers	'299					●	●	
			●	▲				3
Quadruple Bus-Buffer Registers	'173	●				A		2
Octal Storage Register	'396					●		

PROGRAMMABLE LOGIC ARRAYS

DESCRIPTION	INPUTS	OUTPUTS		TYPE NO	NO. OF PINS	VOLUME
		NO.	TYPE			
Fixed-OR Arrays	16	8	Active-Low	'PAL16L8	20	4
		8	Registered	'PAL16R8		
		6		'PAL16R6		
		4		'PAL16R4		
	19 Registered ▲	8	Active-Low	'PALR19L8	24	
		8	Registered	'PALR19R8		
		6		'PALR19R6		
		4		'PALR19R4		
	19 Latched ▲	8	Active-Low	'PALT19L8	24	
		8	Registered	'PALT19R8		
		6		'PALT19R6		
		4		'PALT19R4		
	20 ▲	8	Active-Low	'PAL20L8	24	
		8	Registered	'PAL20R8		
		6		'PAL20R6		
		4		'PAL20R4		
Field-Programmable 14×32×6 Logic Arrays	14	6	3-State	'PL839	24	
			OC	'PL840		

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COUNTERS

SYNCHRONOUS COUNTERS – POSITIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	STD TTL	ALS	AS	L	LS	S	VOLUME
			TECHNOLOGY						
Decade	Sync	'160	●				A		2
				A	▲				3
	Sync	'162	●				A	●	2
				A	▲				3
	Sync	'560		A					
	Sync	'668					●		2
	Sync	'690					●		
	Sync	'692					●		
Decade Up/Down	Sync	'168					B	●	
				A	▲				3
	Async	'190	●				●		2
				●					3
	Async	'192	●			●	●		2
				●					3
	Sync	'568		A					
	Sync	'696					●		2
	Sync	'698					●		
Decade Rate Multipler, $\frac{1}{N10}$	Async Set-to-9	'167	●						
4-Bit Binary	Sync	'161	●				A		
				A	▲				3
	Sync	'163	●				A	●	2
				A	▲				3
	Sync	'561		A					
	Sync	'669					●		2
	Sync	'691					●		
	Sync	'693					●		
4-Bit Binary Up/Down	Sync	'169					B	●	
				A	▲				3
	Async	'191	●				●		2
				●					3
	Async	'193	●			●	●		2
				●					3
	Sync	'569		A					
	Sync	'697					●		2
	Sync	'699					●		
6-Bit Binary Rate Multipler, $\frac{1}{N2}$		'97	●						
8-Bit Up/Down	Async CLR	'867			●				3
	Sync CLR	'869			●				

ASYNCHRONOUS COUNTERS (RIPPLE CLOCK) – NEGATIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	STD TTL	ALS	AS	L	LS	S	VOLUME
			TECHNOLOGY						
Decade	Set-to-9	'90	A			●	●		2
		'68					●		
	Yes	'176	●						
	Yes	'196	●				●	●	
	Set-to-9	'290	●				●		
4-Bit Binary	None	'93	A			●	●		
		'69					●		
	Yes	'177	●						
	Yes	'197	●				●	●	
	None	'293	●				●		
Divide-by-12	None	'92	A				●		
Dual Decade	None	'390	●				●		
	Set-to-9	'490	●				●		
Dual 4-Bit Binary	None	'393	●				●		

8-BIT BINARY COUNTERS WITH REGISTERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	ALS	AS	LS	VOLUME
			TECHNOLOGY			
Parallel Register Outputs	3-State	'590			●	2
	OC	'591			●	
Parallel Register Inputs	2-State	'592			●	
Parallel I/O	3-State	'593			●	

FREQUENCY DIVIDERS, RATE MULTIPLIERS

DESCRIPTION	TYPE	STD TTL	ALS	AS	LS	VOLUME
		TECHNOLOGY				
50-to-1 Frequency Divider	'56				●	2
60-to-1 Frequency Divider	'57				●	
60-Bit Binary Rate Multiplier,	'97	●				
Decade Rate Multiplier,	'167	●				

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DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS AND SHIFTERS

DATA SELECTORS/MULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY						VOLUME
			STD TTL	ALS	AS	L	LS	S	
16 -To-1	2-State	'150	●						2
	3-State	'250			▲				3
	3-State	'850			▲				
	3-State	'851			▲				
Dual 8-To-1	3-State	'351	●						2
8-To-1	2-State	'151	A				●	●	
				●	●				3
	2-State	'152	A				●		2
	3-State	'251	●				●	●	
				●	▲				3
	3-State	'354					●		2
	2-State	'355					●		
	3-State	'356					●		
	OC	'357					●		
Dual 4-To-1	2-State	'153	●			●	●	●	
				●	●				3
	3-State	'253					●	●	2
				●	●				3
	2-State	'352					●		2
				●	●				3
	3-State	'353					●		2
				●	●				3
Octal 2-To-1 with Storage	3-State	'604					●		2
	OC	'605					●		
	3-State	'606					●		
	OC	'607					●		
Quad 2-To-1 with Storage	2-State	'98				●			
	2-State	'298	●				●		2
					▲				3
	2-State	'398					●		2
	2-State	'399					●		
Quad 2-To-1	2-State	'157	●			●	●	●	
				●	●				3
	2-State	'158					●	●	2
				●	●				3
	3-State	'257					B	●	2
				●	●				3
	3-State	'258					B	●	2
				●	●				3
6-to-1 Universal Multiplexer	3-State	'857		●	●				

DECODERS/DEMULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY						VOLUME
			STD TTL	ALS	AS	L	LS	S	
4-To-16	3-State	'154	●			●			2
	OC	'159	●						
4-To-10 BCD-To-Decimal	2-State	'42	A			●	●		
4-To-10 Excess 3-To-Decimal	2-State	'43	A			●			
4-To-10 Excess 3-Gray-To-Decimal	2-State	'44	A			●			
3-To-8 with Address Latches	2-State	'131		●	▲				3
		'137		●	▲				
							●		2
3-To-8	2-State	'138		●	▲				3
							●	●	2
	3-State	'538		▲					3
Dual 2-To-4	2-State	'139		▲	●				
							A	●	2
	2-State	'155	●				A		
	OC	'156	●				●		
Dual 1-To-4 Decoders	3-State	'539		▲					3

CODE CONVERTERS

DESCRIPTION	TYPE	TECHNOLOGY		VOLUME
		STD TTL	S	
6-Line-BCD to 6-Line Binary, Or 4-Line to 4-Line BCD 9's/BCD 10's Converters	'184	●		2
6-Bit-Binary to 6-Bit BCD Converters	'185	A		
BCD-to-Binary Converters	'484		A	4
Binary-to-BCD Converters	'485		A	

PRIORITY ENCODERS/REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	LS	
Full BCD	'147	●			●	2
Cascadable Octal	'148	●			●	
Cascadable Octal with 3-State Outputs	'348				●	
4-Bit Cascadable with Registers	'278	●				

SHIFTERS

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY						VOLUME
			STD TTL	ALS	AS	L	LS	S	
4-Bit Shifter	3-State	'350						●	2
Parallel 16-Bit Multi-Mode Barrel Shifter	3-State	'897			▲				4

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DISPLAY DECODERS/DRIVERS, MEMORY/MICROPROCESSOR CONTROLLERS, AND VOLTAGE-CONTROLLED OSCILLATORS

OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS

DESCRIPTION	OFF-STATE OUTPUT VOLTAGE	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	L	LS	
BCD-To-Decimal	30 V	'45	●					2
	60 V	'141	●					
	15 V	'145	●				●	
	7 V	'445					●	
BCD-To-Seven-Segment	30 V	'46	A			●		
	15 V	'47	A			●	●	
	5.5 V	'48	●				●	
	5.5 V	'49	●				●	
	30 V	'246	●					
	15 V	'247	●				●	
	7 V	'347					●	
	7 V	'447					●	
	5.5 V	'248	●				●	
	5.5 V	'249	●				●	

OPEN COLLECTOR DISPLAY DECODERS/DRIVERS WITH COUNTERS/LATCH

DESCRIPTION	TYPE	TECHNOLOGY			VOLUME
		STD TTL	ALS	AS	
BCD Counter/4-Bit Latch/BCD-To-Decimal Decoder/Driver	'142	●			2
BCD Counter/4-Bit Latch/BCD-To-Seven-Segment Decoder/Lad Driver	'143	●			
BCD Counter/4-Bit Latch/BCD-To-Seven-Segment Decoder/Lamp Driver	'144	●			

VOLTAGE-CONTROLLED OSCILLATORS

DESCRIPTION						TYPE	TECHNOLOGY		VOLUME
No. VCO'S	COMP'L Z_{OUT}	ENABLE	RANGE INPUT	R_{ext}	f_{max} MHz		LS	S	
Single	Yes	Yes	Yes	No	20	'624	●		2
Single	Yes	Yes	Yes	Yes	20	'628	●		
Dual	No	Yes	Yes	No	60	'124		●	
Dual	Yes	Yes	No	No	20	'626	●		
Dual	No	No	No	No	20	'627	●		
Dual	No	Yes	Yes	No	20	'629	●		

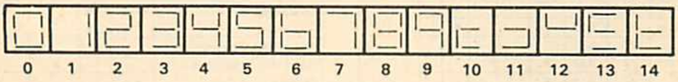
MEMORY/MICROPROCESSOR CONTROLLERS

DESCRIPTION			TYPE	TECHNOLOGY				VOLUME
				ALS	AS	LS	S	
System Controllers For 8080A			'428				●	4
System Controller, Universal			'482				●	
System Controllers, Universal			'890		▲			
(or For '888, '889)			'891		▲			
Memory Refresh Controllers	Transparent, Burst Modes	4K, 16K	'600			A		2
		64K	'601			A		
	Cycle Steal, Burst Modes	4K, 16K	'602			A		
		64K	'603			A		
Memory Cycle Controller			'608			●		
Memory Mappers		3-State	'612			●		
		OC	'613			●		
Memory Mappers With Output Latches		3-State	'610			●		
		OC	'611			●		
Multi-Mode Latches (8080A Applications)			'412				●	

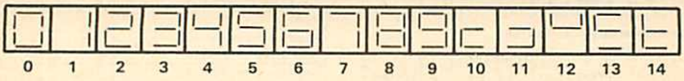
CLOCK GENERATOR CIRCUITS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Quadruple Complementary-Output Logic Elements	'265	●					2
Dual Pulse Synchronizers/Drivers	'120	●					
Crystal-Controlled Oscillators	'320				●		
	'321				●		
Digital Phase-Lock Loop	'297				●		
Programmable Frequency Dividers/Digital Timers	'292				●		
	'294				●		
Triple 4-Input AND/NAND Drivers	'800			▲			3
Triple 4-Input OR/NOR Drivers	'802			▲			
Dual VCO	'124					●	2

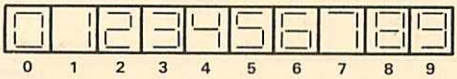
RESULTANT DISPLAYS USING '46A, '47A, '48, '49, 'L46, 'L47, 'LS47, 'LS48, 'LS49, 'LS347



RESULTANT DISPLAYS USING '246, '247, '248, '249, 'LS247, 'LS248, 'LS249, 'LS447



RESULTANT DISPLAYS USING '143, '144



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ARITHMETIC CIRCUITS, ERROR DETECTION CIRCUITS, AND PROCESSOR ELEMENTS

4-BIT COMPARATORS

DESCRIPTION					TYPE	TECHNOLOGY						VOLUME
P = Q	P > Q	P < Q	OUTPUT	OUTPUT ENABLE		STD TTL	ALS	AS	L	LS	S	
Yes	Yes	No	2-State	Yes	'85	●			●	●	●	2

8-BIT COMPARATORS

DESCRIPTION							TYPE	TECHNOLOGY			VOLUME
INPUTS	P = Q	$\overline{P = Q}$	P > Q	P > Q	OUTPUT	OUTPUT ENABLE		ALS	AS	LS	
20 kΩ Pull-Up	Yes	No	No	No	OC	Yes	'518	●			3
	No	Yes	No	No	2-State	Yes	'520	●			
	No	Yes	No	No	OC	Yes	'522	●			
	Yes	No	Yes	No	2-State	No	'682			●	2
	Yes	No	Yes	No	OC	No	'683			●	
Standard	Yes	No	No	No	OC	Yes	'519	●			3
	No	Yes	No	No	2-State	Yes	'521	●			
	Yes	No	Yes	No	2-State	No	'684			●	2
	Yes	No	Yes	No	OC	No	'685			●	
	Yes	No	Yes	No	2-State	Yes	'686			●	
	Yes	No	Yes	No	OC	Yes	'687			●	
	No	Yes	No	Yes	2-State	Yes	'688	●			3
										●	2
	No	Yes	No	No	OC	Yes	'689	●			3
										●	2
Latched P	No	No	Yes	Yes	2-State	Yes	'885		●		3
Latched P and Q	Yes	No	Yes	Yes	Latched	Yes	'866		●		

ADDRESS COMPARATORS

DESCRIPTION	OUTPUT ENABLE	LATCHED OUTPUT	TYPE	TECHNOLOGY		VOLUME
				ALS	AS	
16-Bit to 4-Bit	Yes		'677	●		3
		Yes	'678	▲		
12-Bit to 4-Bit	Yes		'679	●		
		Yes	'680	▲		

PARITY GENERATORS/CHECKERS, ERROR DETECTION AND CORRECTION CIRCUITS

DESCRIPTION		NO. OF BITS	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
Odd/Even Parity Generators/Checkers		8	'180	●					2
		9	'260			●	●		
						▲			3
		9	'286			▲			3
Parallel Error Detection/Correction Circuits	3-State	8	'636				●		2
	OC	8	'637				●		
	3-State	16	'630				●		
	OC	16	'631				●		
	3-State	32	'632	●					3
	OC	32	'633	▲					
	3-State	32	'634	▲					
	OC	32	'635	▲					

FUSE-PROGRAMMABLE COMPARATORS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
16-Bit Identity Comparator	'526		▲				3
12-Bit identity Comparator	'528		▲				
8-Bit Identity Comparator and 4-Bit Comparator	'527		▲				

PARALLEL BINARY ADDERS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
1-Bit Gated	'80	●						2
2-Bit	'82	●						
4-Bit	'83	A				A		
	'283	●				●	●	
Dual 1-Bit Carry-Save	'183				●	●		

ACCUMULATORS, ARITHMETIC LOGIC UNITS, LOOK-AHEAD CARRY GENERATORS

DESCRIPTION		TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	LS	S	
4-Bit Parallel Binary Accumulators		'281					●	2
		'681				●		
4-Bit Arithmetic Logic Units/ Function Generators		'181	●			●	●	
					A			3
		'381				A		2
							●	
		'881			A			3
4-Bit Arithmetic Logic Unit with Ripple Carry		'382				●		2
Look-Ahead Carry Generators	16-Bit	'182	●				●	2
					▲			3
		'282			▲			
	32-Bit	'882			●			3
Quad Serial Adder/Subtractor		'385				●		2
4-Bit Slice Elements		'481				●	●	4
8-Bit Slice Elements		'888			▲			
		'889			▲			

MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
2-Bit-by-4-Bit Parallel Binery Multipliers	'261				●		2
4-Bit-by-4-Bit Parallel Binary Multipliers	'274					●	
	'284	●					
	'285	●					
25-MHz 6-Bit Binary Rate Multipliers	'97	●					
25-MHz Decade Rate Multipliers	'167	●					
8-Bit × 1-Bit 2's Complement Multipliers	'384				●		
16-Bit Parallel Multiplier	'1616		▲				4

OTHER ARITHMETIC OPERATORS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Quad 2-Input Exclusive-OR Gates with Totem-Pole Outputs	'86	●				●	A	●	2
			▲						3
	'386						A		2
Quad 2-Input Exclusive-OR Gates with Open-Collector Outputs	'136	●					●		
Quad 2-Input Exclusive-NOR Gates	'266						●		
Quad Exclusive OR/NOR Gates	'135							●	
4-Bit True/Complement, Element	'87				●				

BIPOLAR BIT-SLICE PROCESSOR ELEMENTS

DESCRIPTION	CASCADABLE TO N-BITS	TYPE	TECHNOLOGY				VOLUME
			ALS	AS	LS	S	
4-Bit-Slice	Yes	'481			●	●	4
8-Bit-Slice	Yes	'888		▲			
	Yes	'889		▲			

●Denotes available tchnology.
▲Denotes planned new products.
A Denotes "A" suffix version available in the technology indicated.

MEMORIES

USER-PROGRAMMABLE READ-ONLY MEMORIES (PROM's)
STANDARD PROM's

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	VOLUME
16K-Bit Arrays	▲ TBP28S165	2048W × 8B	3-State	4
	TBP28S166	2048W × 8B	3-State	
8K-Bit Arrays	TBP24S81	2048W × 4B	3-State	
	TBP24SA81	2048W × 4B	OC	
	TBP28S86A	1024W × 8B	3-State	
	TBP28SA86A	1024W × 8B	OC	
	▲ TBP28S85A	1024W × 8B	3-State	
4K-Bit Arrays	TBP28S42	512W × 8B	3-State	
	TBP28SA42	512W × 8B	OC	
	▲ TBP28S45	512W × 8B	3-State	
	TBP28S46	512W × 8B	3-State	
	TBP28SA46	512W × 8B	OC	
	TBP24S41	1024W × 4B	3-State	
	TBP24SA41	1024W × 4B	OC	
1K-Bit Arrays	TBP24S10	256W × 4B	3-State	
	TBP24SA10	256W × 4B	OC	
256-Bit Arrays	TBP18S030	32W × 8B	3-State	
	TBP18SA030	32W × 8B	OC	

LOW-POWER PROM's

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	VOLUME
16K-Bit Arrays	▲ TBP28L165	2048W × 8B	3-State	4
	▲ TBP28L166	2048W × 8B	3-State	
8K-Bit Arrays	▲ TBP28L85A	1024W × 8B	3-State	
	TBP28L86A	1024W × 8B	3-State	
4K-Bit Arrays	TBP28L42	512W × 8B	3-State	
	▲ TBP28L45	512W × 8B	3-State	
	TBP28L46	512W × 8B	3-State	
2K-Bit Arrays	TBP28L22	256W × 8B	3-State	
	TBP28LA22	256W × 8B	OC	

READ-ONLY MEMORIES (ROM's)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				VOLUME
				STD TTL	ALS	AS	S	
1024-Bit Arrays	256 × 4	OC	'187	●				4
256-Bit Arrays	32 × 8	OC	'88	A				

RANDOM-ACCESS READ-WRITE MEMORIES (RAM's)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
256-Bit Arrays	256 × 1	3-State	'201					●	4
		OC	'301					●	
64-Bit Arrays	16 × 4	OC	'89	●					
		3-State	'189				A	B	
		3-State	'219				A		
		OC	'289				A	B	
		OC	'319				A		
16-Bit Multiple-Port Register File	8 × 2	3-State	'172	●					2
16-Bit Register File	4 × 4	OC	'170	●			●		
		3-State	'670				●		
Dual 64-Bit Register Files	16 × 4	3-State	'870			●			3
			'871			●			

FIRST-IN FIRST-OUT MEMORIES (FIFO'S)

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				VOLUME
			ALS	AS	LS	LS	
Asynchronous 16 × 5	3-State	'225				●	4
Asynchronous 16 × 4	3-State	'222			●		
	3-State	'224			●		
	OC	'227			●		
	OC	'228			●		

● Denotes available technology.
▲ Denotes planned new products.
A Denotes "A" suffix version available in the technology indicated.

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00

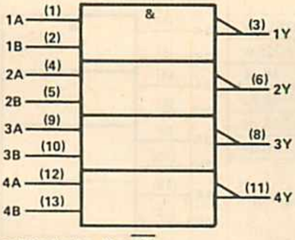
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

typical performance

TYPE	POWER	DELAY
'00	10 mW	10 ns
'ALS00A	1.25 mW	3.5 ns
'AS00	8 mW	3 ns
'H00	22 mW	6 ns
'L00	1 mW	33 ns
'LS00	2 mW	9.5 ns
'S00	19 mW	3 ns

SN5400 (J,FH)	SN7400 (J,N)
SN54ALS00A (J,FH)	SN74ALS00A (N,FN)
SN54AS00 (J,FH)	SN74AS00 (N,FN)
SN54H00 (J)	SN74H00 (J,N)
SN54L00 (J)	
SN54LS00 (J,FH)	SN74LS00 (J,N,FN)
SN54S00 (J,FH)	SN74S00 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

01

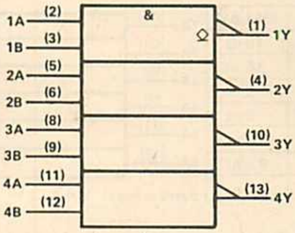
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	POWER	DELAY
'01	10 mW	22 ns
'ALS01	1.28 mW	16 ns
'H01	22 mW	8 ns
'LS01	2 mW	16 ns

SN5401 (J,FH)	SN7401 (J,N)
SN54ALS01 (J,FH)	SN74ALS01 (N,FN)
SN54H01 (J)	SN74H01 (J,N)
SN54LS01 (J,FH)	SN74LS01 (J,N,FN)

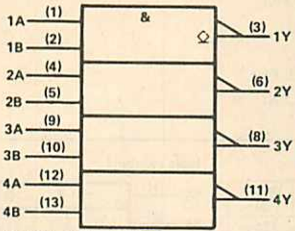
logic symbol, '01, 'ALS01, 'LS01†



pin assignments, '01, 'ALS01, 'LS01

J, N PACKAGES				FH, FN PACKAGES			
1	1Y	8	3A	1	nc	11	nc
2	1A	9	3B	2	1Y	12	3A
3	1B	10	3Y	3	1A	13	3B
4	2Y	11	4A	4	1B	14	3Y
5	2A	12	4B	5	nc	15	nc
6	2B	13	4Y	6	2Y	16	4A
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4B
				9	2B	19	4Y
				10	GND	20	V_{CC}

logic symbol, 'H01†



positive logic: $Y = \overline{AB}$

pin assignments, 'H01

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

02

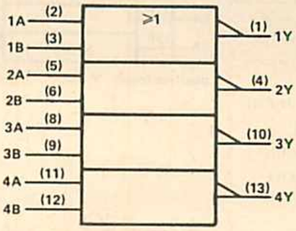
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

typical performance

TYPE	POWER	DELAY
'02	14 mW	10 ns
'ALS02	1.89 mW	5.5 ns
'AS02	12 mW	3 ns
'L02	1.5 mW	33 ns
'LS02	2.75 mW	10 ns
'S02	29 mW	3.5 ns

SN5402 (J,FH)	SN7402 (J,N)
SN54ALS02 (J,FH)	SN74ALS02 (N,FN)
SN54AS02 (J,FH)	SN74AS02 (N,FN)
SN54L02 (J)	
SN54LS02 (J,FH)	SN74LS02 (J,N,FN)
SN54S02 (J,FH)	SN74S02 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A + B}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1Y	8	3A	1	nc	11	nc
2	1A	9	3B	2	1Y	12	3A
3	1B	10	3Y	3	1A	13	3B
4	2Y	11	4A	4	1B	14	3Y
5	2A	12	4B	5	nc	15	nc
6	2B	13	4Y	6	2Y	16	4A
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4B
				9	2B	19	4Y
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection

03

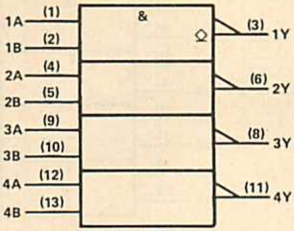
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	POWER	DELAY
'03	10 mW	22 ns
'ALS03A	1.28 mW	16 ns
'L03	1 mW	46 ns
'LS03	2 mW	16 ns
'S03	17.5 mW	16 ns

SN5403 (J,FH)	SN7403 (J,N)
SN54ALS03A (J,FH)	SN74ALS03A (N,FN)
SN54L03 (J)	
SN54LS03 (J,FH)	SN74LS03 (J,N,FN)
SN54S03 (J,FH)	SN74S03 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	nc	15	nc
6	2A	16	4Y
7	nc	17	nc
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

04

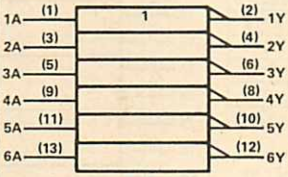
HEX INVERTERS

typical performance

TYPE	POWER	DELAY
'04	10 mW	10 ns
'ALS04A	1.27 mW	3.5 ns
AS04	7.4 mW	3 ns
'H04	22 mW	6 ns
'L04	1 mW	33 ns
'LS04	2 mW	9.5 ns
'S04	19 mW	3 ns

SN5404 (J,FH)	SN7404 (J,N)
SN54ALS04A (J,FH)	SN74ALS04A (N,FN)
SN54AS04 (J,FH)	SN74AS04 (N,FN)
SN54H04 (J)	SN74H04 (J,N)
SN54L04 (J)	
SN54LS04 (J,FH)	SN74LS04 (J,N,FN)
SN54S04 (J,FH)	SN74S04 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2A	14	5Y
5	nc	15	nc
6	2Y	16	5A
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

05

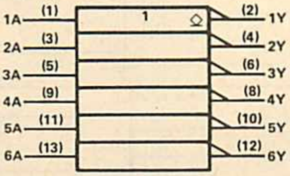
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	POWER	DELAY
'05	10 mW	24 ns
'ALS05A	1.27 mW	13.5 ns
'H05	22 mW	8 ns
'LS05	2 mW	16 ns
'S05	17.5 mW	5 ns

SN5405 (J,FH)	SN7405 (J,N)
SN54ALS05A (J,FH)	SN74ALS05A (N,FN)
SN54H05 (J)	SN74H05 (J,N)
SN54LS05 (J,FH)	SN74LS05 (J,N,FN)
SN54S05 (J,FH)	SN74S05 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2A	14	5Y
5	nc	15	nc
6	2Y	16	5A
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

06

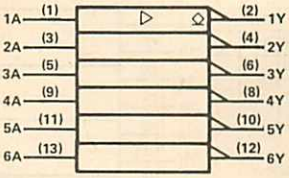
HEX INVERTER BUFFER/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYPICAL POWER PER GATE
SN54'	30 V	30 mA	12.5 ns	26 mW
SN74'	30 V	40 mA	12.5 ns	26 mW

SN5406 (J,FH) SN7406 (J,N)

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2A	14	5Y
5	nc	15	nc
6	2Y	16	5A
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

07

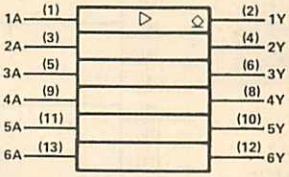
HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYPICAL POWER PER GATE
SN54'	30 V	30 mA	13 ns	21 mW
SN74'	30 V	40 mA	13 ns	21 mW

SN5407 (J,FH) SN7407 (J,N)

logic symbol†



positive logic: $Y = A$

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2A	14	5Y
5	nc	15	nc
6	2Y	16	5A
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

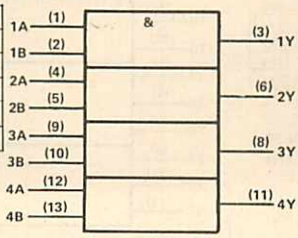
08

QUADRUPLE 2-INPUT POSITIVE-AND GATES

TYPE	POWER	DELAY
'08	19 mW	15 ns
'ALS08	2.19 mW	6.5 ns
AS08	13 mW	4 ns
'LS08	4.25 mW	12 ns
'S08	32 mW	4.75 ns

SN5408 (J,FH) SN7408 (J,N)
SN54ALS08 (J,FH) SN74ALS08 (N,FN)
SN54AS08 (J,FH) SN74AS08 (N,FN)
SN54LS08 (J,FH) SN74LS08 (J,N,FN)
SN54S08 (J,FH) SN74S08 (J,N,FN)

logic symbol†



positive logic: $Y = AB$

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	nc	15	nc
6	2A	16	4Y
7	nc	17	nc
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

09

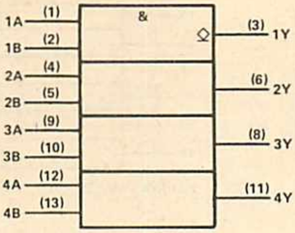
QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

SN5409 (J,FH)	SN7409 (J,N)
SN54ALS09 (J,FH)	SN74ALS09 (N,FN)
SN54LS09 (J,FH)	SN74LS09 (J,N,FN)
SN54S09 (J,FH)	SN74S09 (J,N,FN)

typical performance

TYPE	POWER	DELAY
'09	19.4 mW	18.5 ns
'ALS09	2.22 mW	15 ns
'LS09	4.25 mW	20 ns
'S09	32 mW	6.5 ns

logic symbol†



positive logic: Y = AB

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

10

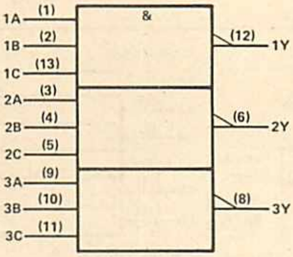
TRIPLE 3-INPUT POSITIVE-NAND GATES

typical performance

TYPE	POWER	DELAY
'10	10 mW	10 ns
'ALS10	1.27 mW	7 ns
'AS10	8 mW	3 ns
'H10	22 mW	6 ns
'L10	1 mW	33 ns
'LS10	2 mW	9.5 ns
'S10	19 mW	3 ns

SN5410 (J,FH)	SN7410 (J,N)
SN54ALS10 (J,FH)	SN74ALS10 (N,FN)
SN54AS10 (J,FH)	SN74AS10 (N,FN)
SN54H10 (J)	SN74H10 (J,N)
SN54L10 (J)	
SN54LS10 (J,FH)	SN74LS10 (J,N,FN)
SN54S10 (J,FH)	SN74S10 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABC}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	2A	10	3B	3	1B	13	3A
4	2B	11	3C	4	2A	14	3B
5	2C	12	1Y	5	nc	15	nc
6	2Y	13	1C	6	2B	16	3C
7	GND	14	V_{CC}	7	nc	17	nc
				8	2C	18	1Y
				9	2Y	19	1C
				10	GND	20	V_{CC}

11

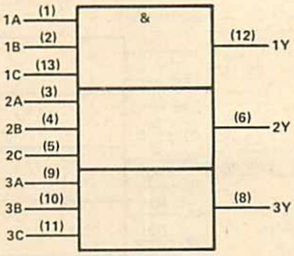
TRIPLE 3-INPUT POSITIVE-AND GATES

typical performance

TYPE	POWER	DELAY
'ALS11	2.17 mW	9 ns
'AS11	13 mW	4 ns
'H11	40 mW	8.2 ns
'LS11	4.25 mW	12 ns
'S11	31 mW	4.75 ns

SN54ALS11 (J,FH)	SN74ALS11 (N,FN)
SN54AS11 (J,FH)	SN74AS11 (N,FN)
SN54H11 (J)	SN74H11 (J,N)
SN54LS11 (J,FH)	SN74LS11 (J,N,FN)
SN54S11 (J,FH)	SN74S11 (J,N,FN)

logic symbol†



positive logic: Y = ABC

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	2A	10	3B	3	1B	13	3A
4	2B	11	3C	4	2A	14	3B
5	2C	12	1Y	5	nc	15	nc
6	2Y	13	1C	6	2B	16	3C
7	GND	14	V_{CC}	7	nc	17	nc
				8	2C	18	1Y
				9	2Y	19	1C
				10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

12

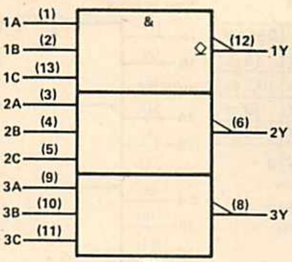
TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

SN5412 (J,FH)	SN7412 (J,N)
SN54ALS12 (J,FH)	SN74ALS12 (N,FN)
SN54LS12 (J,FH)	SN74LS12 (J,N,FN)

typical performance

TYPE	POWER	DELAY
'12	10 mW	22 ns
'ALS12	1.27 mW	17.5 ns
'LS12	2 mW	16 ns

logic symbol†



positive logic: $Y = \overline{ABC}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	2A	10	3B	3	1B	13	3A
4	2B	11	3C	4	2A	14	3B
5	2C	12	1Y	5	nc	15	nc
6	2Y	13	1C	6	2B	16	3C
7	GND	14	V_{CC}	7	nc	17	nc
				8	2C	18	1Y
				9	2Y	19	1C
				10	GND	20	V_{CC}

13

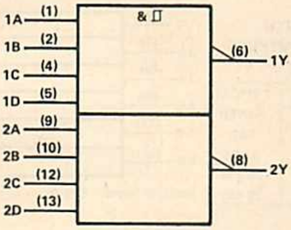
DUAL 4-INPUT POSITIVE-NAND SCHMITT TRIGGERS

SN5413 (J,FH)	SN7413 (J,N)
SN54LS13 (J,FH)	SN74LS13 (J,N,FN)

typical performance

TYPE	HYSTERESIS	DELAY
'13	0.8 V	16.5 ns
'LS13	0.8 V	16.5 ns

logic symbol†



positive logic: $Y = \overline{ABCD}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	2Y	1	nc	11	nc
2	1B	9	2A	2	1A	12	2Y
3	nc	10	2B	3	1B	13	2A
4	1C	11	nc	4	nc	14	2B
5	1D	12	2C	5	nc	15	nc
6	1Y	13	2D	6	1C	16	nc
7	GND	14	V_{CC}	7	nc	17	nc
				8	1D	18	2C
				9	1Y	19	2D
				10	GND	20	V_{CC}

14

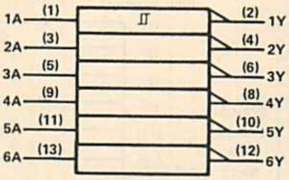
HEX SCHMITT-TRIGGER INVERTERS

SN5414 (J,FH)	SN7414 (J,N)
SN54LS14 (J,FH)	SN74LS14 (J,N,FN)

typical performance

TYPE	HYSTERESIS	DELAY
'14	0.8 V	15 ns
'LS14	0.8 V	15 ns

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	4Y	1	nc	11	nc
2	1Y	9	4A	2	1A	12	4Y
3	2A	10	5Y	3	1Y	13	4A
4	2Y	11	5A	4	2A	14	5Y
5	3A	12	6Y	5	nc	15	nc
6	3Y	13	6A	6	2Y	16	5A
7	GND	14	V_{CC}	7	nc	17	nc
				8	3A	18	6Y
				9	3Y	19	6A
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

15

TRIPLE 3-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

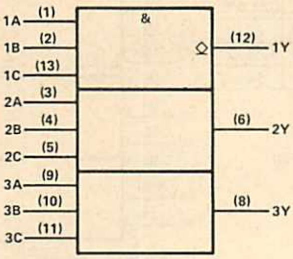
typical performance

TYPE	POWER	DELAY
'ALS15	2.22 mW	15 ns
'H15	38 mW	10.5 ns
'LS15	4.25 mW	15 ns
'S15	28 mW	15 ns

SN54ALS15 (J,FH)
SN54H15 (J)
SN54LS15 (J,FH)
SN54S15 (J,FH)

SN74ALS15 (N,FN)
SN74H15 (J,N)
SN74LS15 (J,N,FN)
SN74S15 (J,N,FN)

logic symbol†



positive logic: Y = ABC

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	2A	10	3B
4	2B	11	3C
5	2C	12	1Y
6	2Y	13	1C
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	2A	14	3B
5	nc	15	nc
6	2B	16	3C
7	nc	17	nc
8	2C	18	1Y
9	2Y	19	1C
10	GND	20	V_{CC}

16

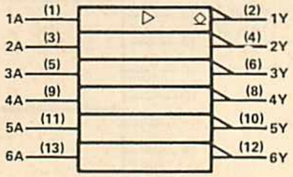
HEX INVERTER BUFFER/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYPICAL POWER PER GATE
SN74'	15 V	40 mA	12.5 ns	26 mW
SN54'	15 V	30 mA	12.5 ns	26 mW

SN5416 (J) SN7416 (J,N)

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

17

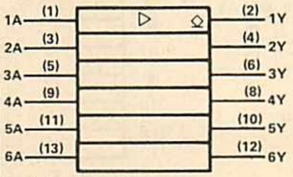
HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYPICAL POWER PER GATE
SN74'	15 V	40 mA	13 ns	21 mW
SN54'	15 V	30 mA	13 ns	21 mW

SN5417 (J) SN7417 (J,N)

logic symbol†



positive logic: Y = A

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

18

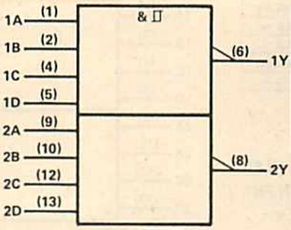
SCHMITT-TRIGGER POSITIVE-NAND GATES WITH TOTEM-POLE OUTPUTS

SN54LS18 (J,FH) SN74LS18 (J,N,FN)

typical performance

TYPE	HYSTERESIS	DELAY
'LS18	0.7 V	25 ns

logic symbol†



positive logic: $Y = \overline{ABCD}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	2Y	1	nc	11	nc
2	1B	9	2A	2	1A	12	2Y
3	nc	10	2B	3	1B	13	2A
4	1C	11	nc	4	nc	14	2B
5	1D	12	2C	5	nc	15	nc
6	1Y	13	2D	6	1C	16	nc
7	GND	14	V_{CC}	7	nc	17	nc
				8	1D	18	2C
				9	1Y	19	2D
				10	GND	20	V_{CC}

19

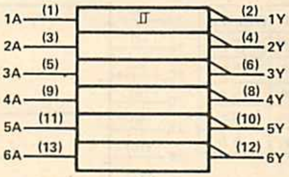
SCHMITT-TRIGGER INVERTERS WITH TOTEM-POLE OUTPUTS

SN54LS19 (J,FH) SN74LS19 (J,N,FN)

typical performance

TYPE	HYSTERESIS	DELAY
'LS19	0.7 V	16 ns

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	4Y	1	nc	11	nc
2	1Y	9	4A	2	1A	12	4Y
3	2A	10	5Y	3	1Y	13	4A
4	2Y	11	5A	4	2A	14	5Y
5	3A	12	6Y	5	nc	15	nc
6	3Y	13	6A	6	2Y	16	5A
7	GND	14	V_{CC}	7	nc	17	nc
				8	3A	18	6Y
				9	3Y	19	6A
				10	GND	20	V_{CC}

20

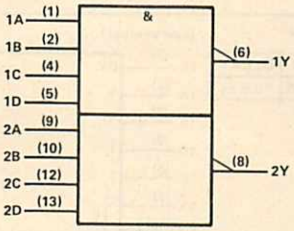
DUAL 4-INPUT POSITIVE-NAND GATES

typical performance

TYPE	POWER	DELAY
'20	10 mW	10 ns
'ALS20A	1.29 mW	4 ns
'AS20	8 mW	3.3 ns
'H20	22 mW	6 ns
'L20	1 mW	33 ns
'LS20	2 mW	9.5 ns
'S20	19 mW	3 ns

SN5420 (J,FH) SN7420 (J,N)
SN54ALS20A (J,FH) SN74ALS20A (N,FN)
SN54AS20 (J,FH) SN74AS20 (N,FN)
SN54H20 (J) SN74H20 (J,N)
SN54L20 (J)
SN54LS20 (J,FH) SN74LS20 (J,N,FN)
SN54S20 (J,FH) SN74S20 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABCD}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	2Y	1	nc	11	nc
2	1B	9	2A	2	1A	12	2Y
3	nc	10	2B	3	1B	13	2A
4	1C	11	nc	4	nc	14	2B
5	1D	12	2C	5	nc	15	nc
6	1Y	13	2D	6	1C	16	nc
7	GND	14	V_{CC}	7	nc	17	nc
				8	1D	18	2C
				9	1Y	19	2D
				10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

21

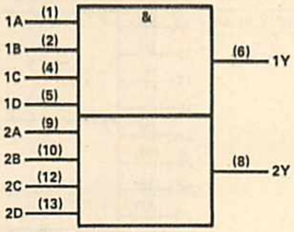
DUAL 4-INPUT POSITIVE-AND GATES

typical performance

TYPE	POWER	DELAY
'ALS21	2.21 mW	8.5 ns
'AS21	13 mW	4.3 ns
'H21	40 mW	8.2 ns
'LS21	4.25 mW	12 ns

SN54ALS21 (J,FH)	SN74ALS21 (N,FN)
SN54AS21 (J,FH)	SN74AS21 (N,FN)
SN54H21 (J)	SN74H21 (J,N)
SN54LS21 (J,FH)	SN74LS21 (J,N,FN)

logic symbol†



positive logic: Y = ABCD

pin assignments

J, N PACKAGES			
1	1A	8	2Y
2	1B	9	2A
3	nc	10	2B
4	1C	11	nc
5	1D	12	2C
6	1Y	13	2D
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	2Y
3	1B	13	2A
4	nc	14	2B
5	nc	15	nc
6	1C	16	nc
7	nc	17	nc
8	1D	18	2C
9	1Y	19	2D
10	GND	20	V_{CC}

22

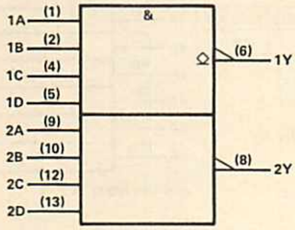
DUAL 4-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	POWER	DELAY
'22	10 mW	22 ns
'ALS22A	1.28 mW	16.5 ns
'H22	22 mW	8 ns
'LS22	2 mW	16 ns
'S22	17.5 mW	5 ns

SN5422 (J,FH)	SN7422 (J,N)
SN54ALS22A (J,FH)	SN74ALS22A (N,FN)
SN54H22 (J)	SN74H22 (J,N)
SN54LS22 (J,FH)	SN74LS22 (J,N,FN)
SN54S22 (J,FH)	SN74S22 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABCD}$

pin assignments

J, N PACKAGES			
1	1A	8	2Y
2	1B	9	2A
3	nc	10	2B
4	1C	11	nc
5	1D	12	2C
6	1Y	13	2D
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	2Y
3	1B	13	2A
4	nc	14	2B
5	nc	15	nc
6	1C	16	nc
7	nc	17	nc
8	1D	18	2C
9	1Y	19	2D
10	GND	20	V_{CC}

23

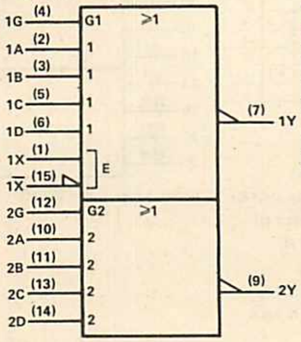
EXPANDABLE DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

typical performance

TYPE	POWER	DELAY
'23	23 mW	10.5 ns

SN5423 (J,FH)	SN7423 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1X	9	2Y
2	1A	10	2A
3	1B	11	2B
4	1G	12	2G
5	1C	13	2C
6	1D	14	2D
7	1Y	15	$1\overline{X}$
8	GND	16	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	1X	12	2Y
3	1A	13	2A
4	1B	14	2B
5	1G	15	2G
6	nc	16	nc
7	1C	17	2C
8	1D	18	2D
9	1Y	19	$1\overline{X}$
10	GND	20	V_{CC}

positive logic:

$1Y = \overline{1G\ (1A+1B+1C+1D)+X}$

$2Y = 2G\ \overline{(2A+2B+2C+2D)}$

X = output of SN5460/SN7460

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

24

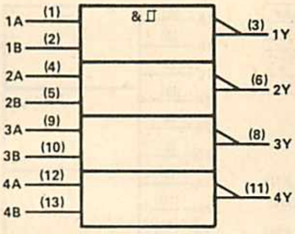
SCHMITT-TRIGGER POSITIVE-NAND GATES/INVERTERS WITH TOTEM POLE OUTPUTS

typical performance

TYPE	HYSTERESIS	DELAY
'LS24	0.7 V	19 ns

SN54LS24 (J,FH) SN74LS24 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	nc	15	nc
6	2A	16	4Y
7	nc	17	nc
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

25

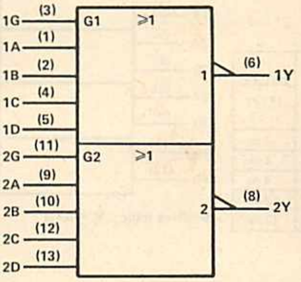
DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

typical performance

TYPE	POWER	DELAY
'25	23 mW	10.5 ns

SN5425 (J,FH) SN7425 (J,N)

logic symbol†



positive logic:
$Y = \overline{G\ (A+B+C+D)}$

pin assignments

J, N PACKAGES			
1	1A	8	2Y
2	1B	9	2A
3	1G	10	2B
4	1C	11	2G
5	1D	12	2C
6	1Y	13	2D
7	GND	14	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	1A	12	2Y
3	1B	13	2A
4	1G	14	2B
5	nc	15	nc
6	1C	16	2G
7	nc	17	nc
8	1D	18	2C
9	1Y	19	2D
10	GND	20	V_{CC}

26

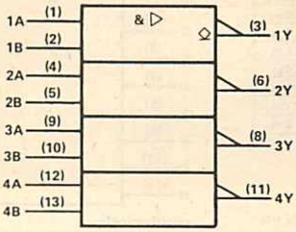
QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	POWER	DELAY
'26	15 V	16 mA	10 mW	13.5 ns
'LS26	15 V	4 mA	2 mW	16 ns

SN5426 (J,FH) SN7426 (J,N)
SN54LS26 (J,FH) SN74LS26 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	nc	15	nc
6	2A	16	4Y
7	nc	17	nc
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

27

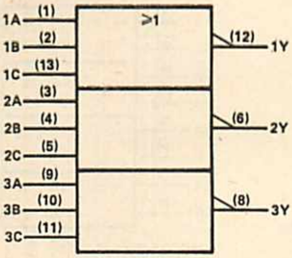
TRIPLE 3-INPUT POSITIVE-NOR GATES

typical performance

TYPE	POWER	DELAY
'27	22 mW	8.5 ns
'ALS27	2.48 mW	6 ns
'AS27	12.2 mW	3.5 ns
'LS27	4.5 mW	10 ns

SN5427 (J,FH)	SN7427 (J,N)
SN54ALS27 (J,FH)	SN74ALS27 (N,FN)
SN54AS27 (J,FH)	SN74AS27 (N,FN)
SN54LS27 (J,FH)	SN74LS27 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A+B+C}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	2A	10	3B	3	1B	13	3A
4	2B	11	3C	4	2A	14	3B
5	2C	12	1Y	5	nc	15	nc
6	2Y	13	1C	6	2B	16	3C
7	GND	14	V_{CC}	7	nc	17	nc
				8	2C	18	1Y
				9	2Y	19	1C
				10	GND	20	V_{CC}

28

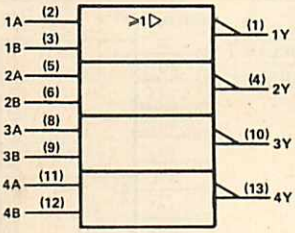
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	POWER (TYP)	DELAY (TYP)
'28	48 mA	−2.4 mA	28 mW	7 ns
SN54ALS'	12 mA	−1 mA	4.06 mW	4 ns
SN74ALS'	24 mA	−2.6 mA	4.06 mW	4 ns
SN54LS'	12 mA	−1.2 mA	5.5 mW	12 ns
SN74LS'	24 mA	−1.2 mA	5.5 mW	12 ns

SN5428 (J,FH)	SN7428 (J,N)
SN54ALS28A (J,FH)	SN74ALS28A (N,FN)
SN54LS28 (J,FH)	SN74LS28 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A+B}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1Y	8	3A	1	nc	11	nc
2	1A	9	3B	2	1Y	12	3A
3	1B	10	3Y	3	1A	13	3B
4	2Y	11	4A	4	1B	14	3Y
5	2A	12	4B	5	nc	15	nc
6	2B	13	4Y	6	2Y	16	4A
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4B
				9	2B	19	4Y
				10	GND	20	V_{CC}

30

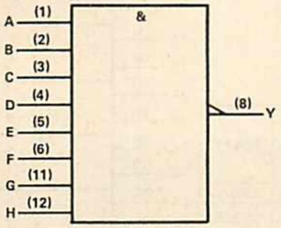
8-INPUT POSITIVE-NAND GATE

typical performance

TYPE	POWER	DELAY
'30	10 mW	10 ns
'ALS30	1.9 mW	7 ns
'AS30	9.75 mW	3.5 ns
'H30	22 mW	6 ns
'L30	1 mW	33 ns
'LS30	2.4 mW	17 ns
'S30	19 mW	3 ns

SN5430 (J,FH)	SN7430 (J,N)
SN54ALS30 (J,FH)	SN74ALS30 (N,FN)
SN54AS30 (J,FH)	SN74AS30 (N,FN)
SN54H30 (J)	SN74H30 (J,N)
SN54L30 (J)	
SN54LS30 (J,FH)	SN74LS30 (J,N,FN)
SN54S30 (J,FH)	SN74S30 (J,N,FN)

logic symbol†



positive logic:
$Y = \overline{ABCDEFGH}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A	8	Y	1	nc	11	nc
2	B	9	nc	2	A	12	Y
3	C	10	nc	3	B	13	nc
4	D	11	G	4	C	14	nc
5	E	12	H	5	nc	15	nc
6	F	13	nc	6	D	16	G
7	GND	14	V_{CC}	7	nc	17	nc
				8	E	18	H
				9	F	19	nc
				10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

31

DELAY ELEMENTS

(delay elements for generating delay lines)

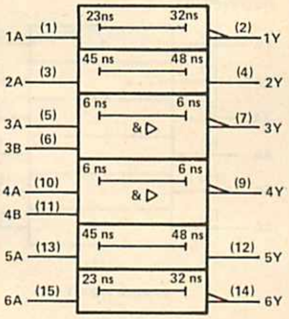
- Buffers 3 and 4 offer 3-fold increase in I_{OL} (12 mA/24 mA)
- Total power dissipation 38 mW

typical performance

DELAY ELEMENT	LOGIC	DELAY
Gates 1 and 6	Inverting	27.5 ns
Gates 2 and 5	Noninverting	46.5 ns
Buffers 3 and 4	2-Input NAND	6 ns

SN54LS31 (J,FH) SN74LS31 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1A	9	4Y
2	1Y	10	4A
3	2A	11	4B
4	2Y	12	5Y
5	3A	13	5A
6	3B	14	6Y
7	3Y	15	6A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2A	14	4B
5	2Y	15	5Y
6	nc	16	nc
7	3A	17	5A
8	3B	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

32

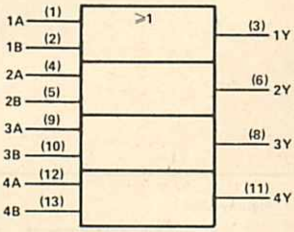
QUADRUPLE 2-INPUT POSITIVE-OR GATE

typical performance

TYPE	POWER	DELAY
'32	24 mW	12 ns
'ALS32	2.81 mW	5.5 ns
'AS32	14.5 mW	4.5 ns
'LS32	5 mW	12 ns
'S32	35 mW	4 ns

SN5432 (J,FH) SN7432 (J,N)
SN54ALS32 (J,FH) SN74ALS32 (N,FN)
SN54AS32 (J,FH) SN74AS32 (N,FN)
SN54LS32 (J,FH) SN74LS32 (J,N,FN)
SN54S32 (J,FH) SN74S32 (J,N,FN)

logic symbol†



positive logic: Y = A+B

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	nc	15	nc
6	2A	16	4Y
7	nc	17	nc
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

33

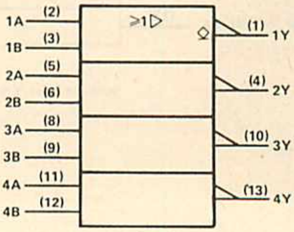
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	POWER (TYP)	DELAY (TYP)
'33	5.5 V	48 mA	28 mW	11 ns
SN54ALS'	5.5 V	12 mA	4.06 mW	14.5 ns
SN74ALS'	5.5 V	24 mA	4.06 mW	14.5 ns
SN54LS'	5.5 V	12 mA	5.45 mW	19 ns
SN74LS'	5.5 V	24 mA	5.45 mW	19 ns

SN5433 (J,FH) SN7433 (J,N)
SN54ALS33A (J,FH) SN74ALS33A (N,FN)
SN54LS33 (J,FH) SN74LS33 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A+B}$

pin assignments

J, N PACKAGES			
1	1Y	8	3A
2	1A	9	3B
3	1B	10	3Y
4	2Y	11	4A
5	2A	12	4B
6	2B	13	4Y
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1Y	12	3A
3	1A	13	3B
4	1B	14	3Y
5	nc	15	nc
6	2Y	16	4A
7	nc	17	nc
8	2A	18	4B
9	2B	19	4Y
10	GND	20	V_{CC}

nc — no internal connection.

†Pin numbers shown on logic symbols are for J and N packages only.

34

HEX NONINVERTERS

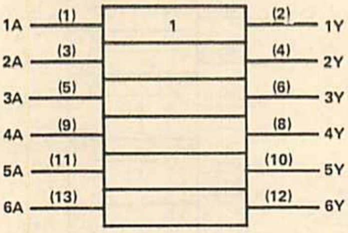
- Non-inverting outputs

typical performance

TYPE	POWER	DELAY
'ALS34	1.9 mW	8 ns
'AS34	12 mW	3.3 ns

SN54ALS34 (J,FH) SN74ALS34 (N,FN)
SN54AS34 (J,FH) SN74AS34 (N,FN)

logic symbol †



positive logic Y = A

pin assignments

J,N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH,FN PACKAGES			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2A	14	5Y
5	nc	15	nc
6	2Y	16	5A
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

35

HEX NONINVERTERS WITH OPEN-COLLECTOR OUTPUTS

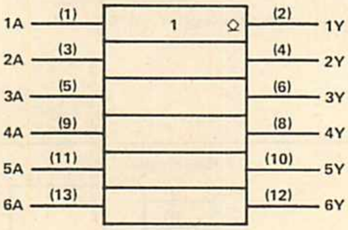
- Non-inverting outputs

typical performance

TYPE	POWER	DELAY
'ALS35	1.9 mW	2.5 ns

SN54ALS35 (J,FH) SN74ALS35 (N,FN)

logic symbol †



positive logic Y = A

pin assignments

J,N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2A	14	5Y
5	nc	15	nc
6	2Y	16	5A
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

37

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

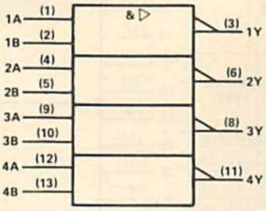
performance

TYPE	HIGH-LEVEL OUTPUT CURRENT	LOW-LEVEL OUTPUT CURRENT	POWER (TYP)	DELAY (TYP)
37	4.8 mA	−1.2 mA	27 mW	10.5 ns
SN54ALS'	12 mA	−1 mA	3.04 mW	4 ns
SN74ALS'	24 mA	−2.6 mA	3.04 mW	4 ns
SN54LS'	12 mA	−1.2 mA	4.3 mW	12 ns
SN74LS'	24 mA	−1.2 mA	4.3 mW	12 ns
'S37	60 mA	−3 mA	41 mW	4 ns

SN5437 (J,FH)
SN54ALS37A (J,FH)
SN54LS37 (J,FH)
SN54S37 (J,FH)

SN7437 (J,N)
SN74ALS37A (N,FN)
SN74LS37 (J,N,FN)
SN74S37 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

38

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

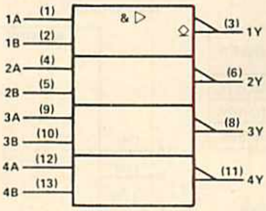
performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	POWER (TYP)	DELAY (TYP)
'38	5.5 V	48 mA	24.4 mW	12.5 ns
SN54ALS'	5.5 V	12 mA	3.04 mW	14.5 ns
SN74ALS'	5.5 V	24 mA	3.04 mW	14.5 ns
SN54ALS'	5.5 V	12 mA	4.3 mW	19 ns
SN74ALS'	5.5 V	24 mA	4.3 mW	19 ns
'S38	5.5 V	60 mA	41 mW	6.5 ns

SN5438 (J,FH)
SN54ALS38A (J,FH)
SN54LS38 (J,FH)
SN54S38 (J,FH)

SN7438 (J,N)
SN74ALS38A (N,FN)
SN74LS38 (J,N,FN)
SN74S38 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

39

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

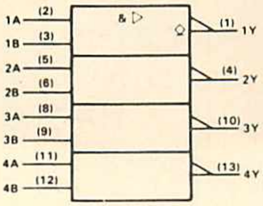
performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	POWER (TYP)	DELAY (TYP)
SN5439	5.5 V	60 mA	24.4 mW	12.5 ns
SN7439	5.5 V	80 mA	24.4 mW	12.5 ns

SN5439 (J,FH)

SN7439 (J,N)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES				FH PACKAGE			
1	1Y	8	3A	1	nc	11	nc
2	1A	9	3B	2	1Y	12	3A
3	1B	10	3Y	3	1A	13	3B
4	2Y	11	4A	4	1B	14	3Y
5	2A	12	4B	5	nc	15	nc
6	2B	13	4Y	6	2Y	16	4A
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4B
				9	2B	19	4Y
				10	GND	20	V_{CC}

nc — no internal connection.

†Pin numbers shown on logic symbols are for J and N packages only.

40

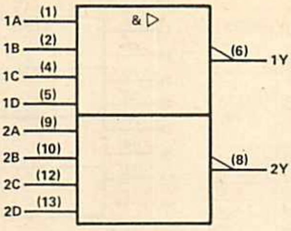
DUAL 4-INPUT POSITIVE NAND BUFFERS

performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	POWER (TYP)	DELAY (TYP)
'40	48 mA	−1.2 mA	26 mW	10.5 ns
SN54ALS'	12 mA	−1 mA	3.04 mW	4 ns
SN74ALS'	24 mA	−2.6 mA	3.04 mW	4 ns
'H40	60 mA	−1.5 mA	44 mW	7.5 ns
SN54LS'	12 mA	−1.2 mA	4.3 mW	12 ns
SN74LS'	24 mA	−1.2 mA	4.3 mW	12 ns
'S40	60 mA	−3 mA	44 mW	4 ns

SN5440 (J,FH)	SN7440 (J,N)
SN54ALS40A (J,FH)	SN74ALS40A (N,FN)
SN54H40 (J)	SN74H40 (J,N)
SN54LS40 (J,FH)	SN74LS40 (J,N,FN)
SN54S40 (J,FH)	SN74S40 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{ABCD}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	2Y	1	nc	11	nc
2	1B	9	2A	2	1A	12	2Y
3	nc	10	2B	3	1B	13	2A
4	1C	11	nc	4	nc	14	2B
5	1D	12	2C	5	nc	15	nc
6	1Y	13	2D	6	1C	16	nc
7	GND	14	V_{CC}	7	nc	17	nc
				8	1D	18	2C
				9	1Y	19	2D
				10	GND	20	V_{CC}

42

4-LINE TO 10-LINE DECODERS

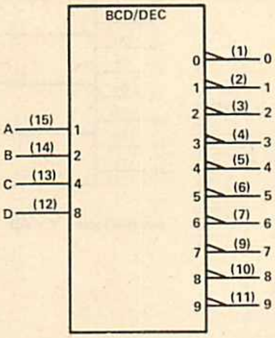
(BCD to decimal)

typical performance

TYPE	SELECT TIME	POWER
'42A	17 ns	140 mW
'L42	34 ns	70 mW
'LS42	17 ns	35 mW

SN5442A (J,FH)	SN7442A (J,N)
SN54L42 (J)	
SN54LS42 (J,FH)	SN74LS42 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	0	9	7	1	nc	11	nc
2	1	10	8	2	0	12	7
3	2	11	9	3	1	13	8
4	3	12	D	4	2	14	9
5	4	13	C	5	3	15	D
6	5	14	B	6	nc	16	nc
7	6	15	A	7	4	17	C
8	GND	16	V_{CC}	8	5	18	B
				9	6	19	A
				10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

43

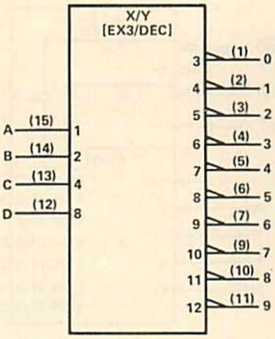
4-LINE TO 10-LINE DECODERS (EXCESS 3 TO DECIMAL)

typical performance

TYPE	SELECT TIME	POWER
'43A	17 ns	140 mW
'L43	34 ns	70 mW

SN5443A (J,FH) SN7443A (J,N)
SN54L43 (J)

logic symbol†



pin assignments

J, N PACKAGES			
1	0	9	7
2	1	10	8
3	2	11	9
4	3	12	D
5	4	13	C
6	5	14	B
7	6	15	A
8	GND	16	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	0	12	7
3	1	13	8
4	2	14	9
5	3	15	D
6	nc	16	nc
7	4	17	C
8	5	18	B
9	6	19	A
10	GND	20	V_{CC}

44

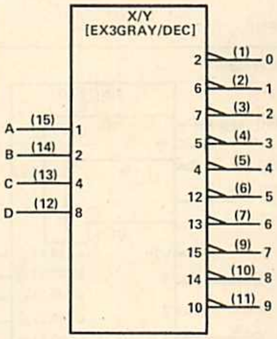
4-LINE TO 10-LINE DECODERS (EXCESS 3-GRAY TO DECIMAL)

typical performance

TYPE	SELECT TIME	POWER
'44A	17 ns	140 mW
'L44	34 ns	70 mW

SN5444A (J,FH) SN7444A (J,N)
SN54L44 (J)

logic symbol†



pin assignments

J, N PACKAGES			
1	0	9	7
2	1	10	8
3	2	11	9
4	3	12	D
5	4	13	C
6	5	14	B
7	6	15	A
8	GND	16	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	0	12	7
3	1	13	8
4	2	14	9
5	3	15	D
6	nc	16	nc
7	4	17	C
8	5	18	B
9	6	19	A
10	GND	20	V_{CC}

45

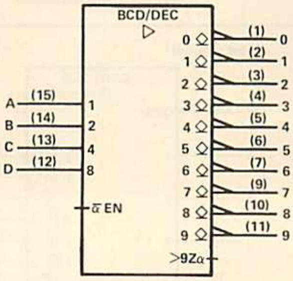
BCD-TO-DECIMAL DECODER/DRIVER

typical performance

TYPE	OFF-STATE OUTPUT VOLTAGE	POWER
'45	30 V	215 mW

SN5445 (J,FH) SN7445 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	0	9	7
2	1	10	8
3	2	11	9
4	3	12	D
5	4	13	C
6	5	14	B
7	6	15	A
8	GND	16	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	0	12	7
3	1	13	8
4	2	14	9
5	3	15	D
6	nc	16	nc
7	4	17	C
8	5	18	B
9	6	19	A
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

46,47

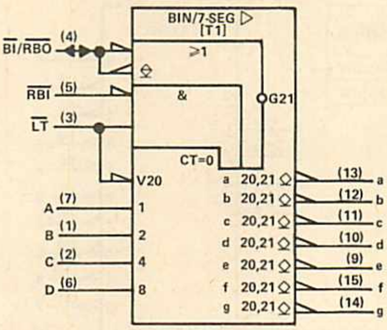
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS
(46 - 30 V OUTPUTS
47 - 15 V OUTPUTS)

typical performance

TYPE	OFF-STATE OUTPUT VOLTAGE	POWER
'46A	30 V	320 mW
'L46	30 V	133 mW
'47A	15 V	320 mW
'L47	15 V	133 mW
'LS47	15 V	35 mW

SN5446A (J,FH) SN7446A (J,N)
SN54L46 (J)
SN5447A (J,FH) SN7447A (J,N)
SN54L47 (J)
SN54LS47 (J,FH) SN74LS47 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	e	1	nc	11	nc
2	C	10	d	2	B	12	e
3	$\overline{LT}$	11	c	3	C	13	d
4	$\overline{BI}/\overline{RBO}$	12	b	4	$\overline{LT}$	14	c
5	$\overline{RBI}$	13	a	5	$\overline{BI}/\overline{RBO}$	15	b
6	D	14	g	6	nc	16	nc
7	A	15	f	7	$\overline{RBI}$	17	a
8	GND	16	V_{CC}	8	D	18	g
				9	A	19	f
				10	GND	20	V_{CC}

48

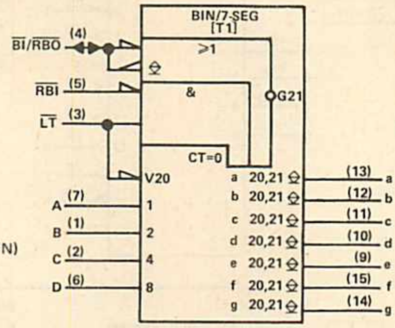
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

typical performance

TYPE	OFF-STATE OUTPUT VOLTAGE	POWER
'48	5.5 V	265 mW
'LS48	5.5 V	125 mW

SN5448 (J,FH) SN7448 (J,N)
SN54LS48 (J,FH) SN74LS48 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	e	1	nc	11	nc
2	C	10	d	2	B	12	e
3	$\overline{LT}$	11	c	3	C	13	d
4	$\overline{BI}/\overline{RBO}$	12	b	4	$\overline{LT}$	14	c
5	$\overline{RBI}$	13	a	5	$\overline{BI}/\overline{RBO}$	15	b
6	D	14	g	6	nc	16	nc
7	A	15	f	7	$\overline{RBI}$	17	a
8	GND	16	V_{CC}	8	D	18	g
				9	A	19	f
				10	GND	20	V_{CC}

49

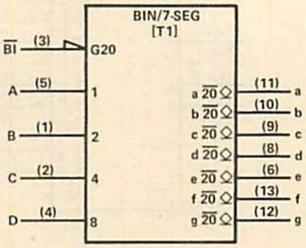
BCD TO SEVEN SEGMENT DECODERS/DRIVERS (OPEN-COLLECTOR OUTPUTS)

typical performance

TYPE	OFF-STATE OUTPUT VOLTAGE	POWER
'49	5.5 V	165 mW
'LS49	5.5 V	40 mW

SN5449 (J,FH) SN7449 (J,N)
SN54LS49 (J,FH) SN74LS49 (J,N,FN)

logic symbol†



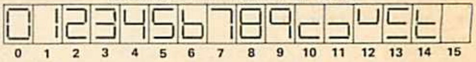
pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	8	d	1	nc	11	nc
2	C	9	c	2	B	12	d
3	$\overline{BI}$	10	b	3	C	13	c
4	D	11	a	4	$\overline{BI}$	14	b
5	A	12	g	5	nc	15	nc
6	e	13	f	6	D	16	a
7	GND	14	V_{CC}	7	nc	17	nc
				8	A	18	g
				9	e	19	f
				10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

FONT TABLE T1 — FOR '46, '47, '48, '49



50

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES (ONE GATE EXPANDABLE)

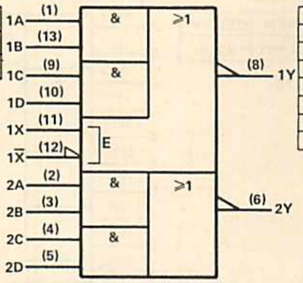
typical performance

TYPE	POWER	DELAY
'50	14 mW	10.5 ns
'H50	29 mW	6.5 ns

SN5450 (J,FH)
SN54H50 (J)

SN7450 (J,N)
SN74H50 (J,N)

logic symbol†



positive logic: $Y = \overline{AB+CD+X}$
'50: X = output of SN5460/SN7460
'H50: X = output of SN54H60/SN74H60
or SN54H62/SN74H62

pin assignments

J, N PACKAGES				FH PACKAGE			
1	1A	8	1Y	1	nc	11	nc
2	2A	9	1C	2	1A	12	1Y
3	2B	10	1D	3	2A	13	1C
4	2C	11	1X	4	2B	14	1D
5	2D	12	$1\overline{X}$	5	nc	15	nc
6	2Y	13	1B	6	2C	16	1X
7	GND	14	V_{CC}	7	nc	17	nc
				8	2D	18	$1\overline{X}$
				9	2Y	19	1B
				10	GND	20	V_{CC}

51

AND-OR INVERT GATES

typical performance

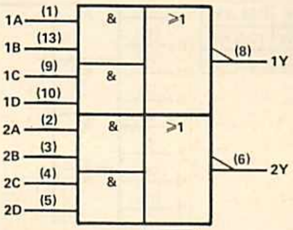
TYPE	POWER	DELAY
'51	14 mW	10.5 ns
'H51	29 mW	65 ns
'L51	1.5 mW	43 ns
'LS51	2.75 mW	12.5 ns
'S51	28 mW	3.5 ns

SN5451 (J,FH)
SN54H51 (J)
SN54L51 (J)
SN54LS51 (J,FH)
SN54S51 (J,FH)

SN7451 (J,N)
SN74H51 (J,N)

SN74LS51(J,N,FN)
SN74S51 (J,N,FN)

logic symbol, '51, 'H51, 'S51†

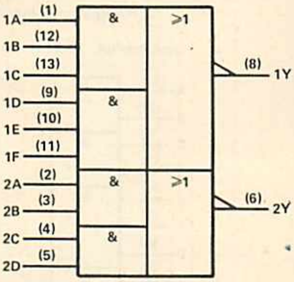


positive logic: $Y = \overline{AB+CD}$

pin assignments, '51, 'H51, 'S51

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	1Y	1	nc	11	nc
2	2A	9	1C	2	1A	12	1Y
3	2B	10	1D	3	2A	13	1C
4	2C	11	nu	4	2B	14	1D
5	2D	12	nu	5	nc	15	nc
6	2Y	13	1B	6	2C	16	nu
7	GND	14	V_{CC}	7	nc	17	nc
				8	2D	18	nu
				9	2Y	19	1B
				10	GND	20	V_{CC}

logic symbol, 'L51, 'LS51†



positive logic:

$1Y = \overline{(1A \cdot 1B \cdot 1C)+(1D \cdot 1E \cdot 1F)}$

$2Y = \overline{(2A \cdot 2B)+(2C \cdot 2D)}$

pin assignments, 'L51, 'LS51

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	1Y	1	nc	11	nc
2	2A	9	1D	2	1A	12	1Y
3	2B	10	1E	3	2A	13	1D
4	2C	11	1F	4	2B	14	1E
5	2D	12	1B	5	nc	15	nc
6	2Y	13	1C	6	2C	16	1F
7	GND	14	V_{CC}	7	nc	17	nc
				8	2D	18	1B
				9	2Y	19	1C
				10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

nu – make no external connection.

52

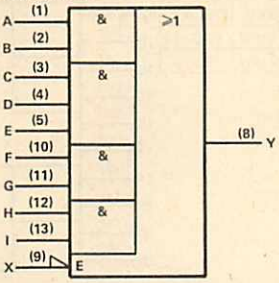
EXPANDABLE 4-WIDE AND-OR GATES

SN54H52 (J,FH) SN74H52 (J,N)

typical performance

TYPE	POWER	DELAY
'H52	88 mW	9.9 ns

logic symbol†



positive logic: $Y = AB+CDE+FG+HI+X$

X = output of SN54H61/SN74H61

pin assignments

J, N PACKAGES				FH PACKAGE			
1	A	8	Y	1	nc	11	nc
2	B	9	X	2	A	12	Y
3	C	10	F	3	B	13	X
4	D	11	G	4	C	14	F
5	E	12	H	5	nc	15	nc
6	nc	13	I	6	D	16	G
7	GND	14	V_{CC}	7	nc	17	nc
				8	E	18	H
				9	nc	19	I
				10	GND	20	V_{CC}

53

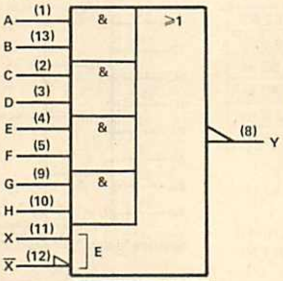
EXPANDABLE 4-WIDE AND-OR-INVERT GATES

SN5453 (J,FH) SN7453 (J,N)
SN54H53 (J) SN74H53 (J,N)

typical performance

TYPE	POWER	DELAY
'53	23 mW	10.5 ns
'H53	41 mW	6.6 ns

logic symbol, '53†



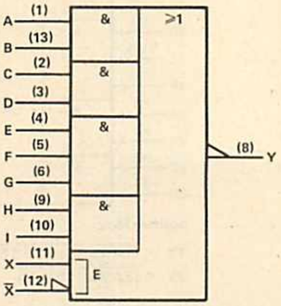
positive logic: $Y = \overline{AB+CD+EF+GH+X}$

X = output of SN5460/SN7460

pin assignments, '53

J, N PACKAGES				FH PACKAGE			
1	A	8	Y	1	nc	11	nc
2	C	9	G	2	A	12	Y
3	D	10	H	3	C	13	G
4	E	11	X	4	D	14	H
5	F	12	$\overline{X}$	5	nc	15	nc
6	nc	13	B	6	E	16	X
7	GND	14	V_{CC}	7	nc	17	nc
				8	F	18	$\overline{X}$
				9	nc	19	B
				10	GND	20	V_{CC}

logic symbol, 'H53†



positive logic: $Y = \overline{AB+CD+EFG+HI+X}$

X = output of SN54H60/SN74H60 or SN54H62/SN74H62

pin assignments, 'H53

J, N PACKAGES			
1	A	8	Y
2	C	9	H
3	D	10	I
4	E	11	X
5	F	12	$\overline{X}$
6	G	13	B
7	GND	14	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

54

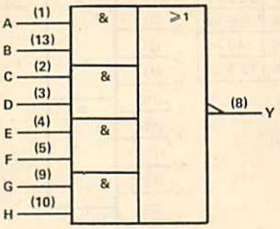
4-WIDE AND-OR-INVERT GATES

typical performance

TYPE	POWER	DELAY
'54	23 mW	10.5 ns
'H54	41 mW	6.6 ns
'L54	1.5 mW	43 ns
'LS54	4.5 mW	12.5 ns

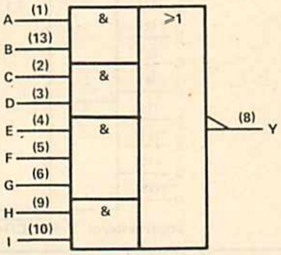
SN5454 (J,FH)	SN7454 (J,N)
SN54H54 (J)	SN74H54 (J,N)
SN54L54 (J)	
SN54LS54 (J,FH)	SN74LS54 (J,N,FN)

logic symbol, '54†



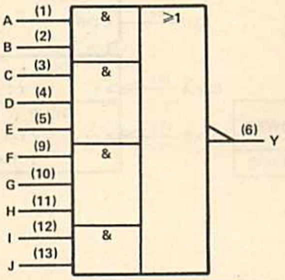
positive logic: $Y = \overline{AB+CD+EF+GH}$

logic symbol, 'H54†



positive logic: $Y = \overline{AB+CD+EFG+HI}$

logic symbol, 'L54, 'LS54†



positive logic: $Y = \overline{AB+CDE+FGH+IJ}$

pin assignments, '54

J, N PACKAGES			
1	A	8	Y
2	C	9	G
3	D	10	H
4	E	11	nu
5	F	12	nu
6	nc	13	B
7	GND	14	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	A	12	Y
3	C	13	G
4	D	14	H
5	nc	15	nc
6	E	16	nu
7	nc	17	nc
8	F	18	nu
9	nc	19	B
10	GND	20	V_{CC}

pin assignments, 'H54

J, N PACKAGES			
1	A	8	Y
2	C	9	H
3	D	10	I
4	E	11	nu
5	F	12	nu
6	G	13	B
7	GND	14	V_{CC}

pin assignments, 'L54, 'LS54

J, N PACKAGES			
1	A	8	nc
2	B	9	F
3	C	10	G
4	D	11	H
5	E	12	I
6	Y	13	J
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	A	12	nc
3	B	13	F
4	C	14	G
5	nc	15	nc
6	D	16	H
7	nc	17	nc
8	E	18	I
9	Y	19	J
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

nu — make no external connection.

55

2-WIDE 4-INPUT AND-OR-INVERT GATES

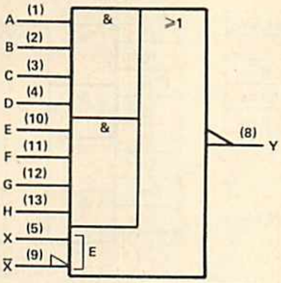
typical performance

TYPE	POWER	DELAY
'H55	30 mW	6.8 ns
'L55	1.5 mW	43 ns
'LS55	2.75 mW	12.5 ns

SN54H55 (J)	SN74H55 (J,N)
SN54L55 (J)	
SN54LS55 (J,FH)	SN74LS55 (J,N,FN)

X = Output of SN54H60/SN74H60 or SN54H62/SN74H62

logic symbol, 'H55†

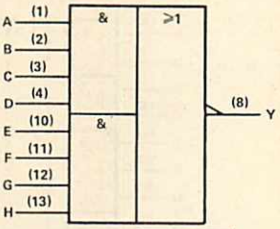


positive logic: $Y = \overline{ABCD+EFGH+X}$

pin assignments, 'H55

J, N PACKAGES			
1	A	8	Y
2	B	9	$\overline{X}$
3	C	10	E
4	D	11	F
5	X	12	G
6	nc	13	H
7	GND	14	V_{CC}

logic symbol, 'L55, 'LS55†



positive logic: $Y = \overline{ABCD+EFGH}$

pin assignments, 'L55, 'LS55

J, N PACKAGES			
1	A	8	Y
2	B	9	nc
3	C	10	E
4	D	11	F
5	nc	12	G
6	nc	13	H
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	A	12	Y
3	B	13	nc
4	C	14	E
5	nc	15	nc
6	D	16	F
7	nc	17	nc
8	nc	18	G
9	nc	19	H
10	GND	20	V_{CC}

56

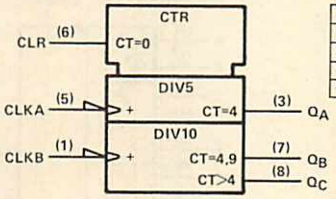
50-TO-1 FREQUENCY DIVIDER

typical performance

TYPE	CLOCK FREQUENCY	CLEAR	POWER
'LS56	25 MHz	HIGH	85 mW

SN54LS56 (JG) SN74LS56 (JG,P)

logic symbol†



pin assignments

JG, P PACKAGES			
1	CLKB	5	CLKA
2	V_{CC}	6	CLR
3	Q_A	7	Q_B
4	GND	8	Q_C

For chip carrier information, contact the factory.

---

†Pin numbers shown on logic symbols are for J, JG, N, and P packages only.

nc — no internal connection.

57

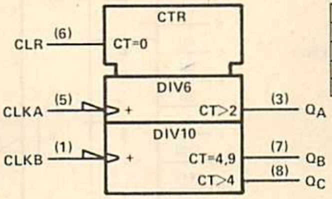
60-TO-1 FREQUENCY DIVIDER

typical performance

TYPE	CLOCK FREQUENCY	CLEAR	POWER
'LS57	25 MHz	HIGH	85 mW

SN54LS57 (JG)   SN54LS57 (JG, P)

logic symbol†



pin assignments

JG, P PACKAGES			
1	CLKB	5	CLKA
2	V_{CC}	6	CLR
3	Q_A	7	Q_B
4	GND	8	Q_C

60

DUAL 4-INPUT EXPANDERS

SN5460 (J)   SN7460 (J,N)
SN54H60 (J)   SN74H60 (J,N)

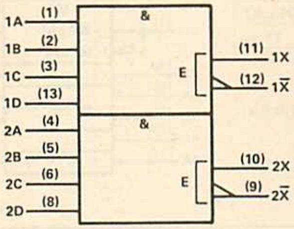
'60 positive logic:
X = ABCD when connected to X and $\overline{X}$ inputs of SN5423/SN7423, SN5450/SN7450, or SN5453/SN7453

'H60 positive logic:
X = ABCD when connected to X and $\overline{X}$ inputs of SN54H50/SN74H50, SN54H53/SN74H53, or SN54H55/SN74H55

typical performance

TYPE	POWER
'60	4 mW
'H60	6 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	1A	8	2D
2	1B	9	$\overline{2X}$
3	1C	10	2X
4	2A	11	1X
5	2B	12	$\overline{1X}$
6	2C	13	1D
7	GND	14	V_{CC}

61

TRIPLE 3-INPUT EXPANDERS

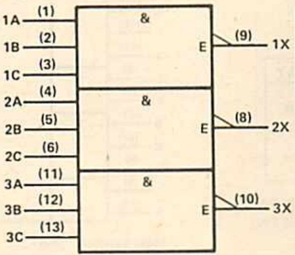
typical performance

TYPE	POWER
'H61	13 mW

SN54H61 (J)   SN74H61 (J,N)

positive logic:
X = ABC when connected to X input of SN54H52/SN74H52

logic symbol†



pin assignments

J, N PACKAGES			
1	1A	8	2X
2	1B	9	1X
3	1C	10	3X
4	2A	11	3A
5	2B	12	3B
6	2C	13	3C
7	GND	14	V_{CC}

† Pin numbers shown on logic symbols are for J, JG, N, and P packages only.
nc – no internal connection.

62

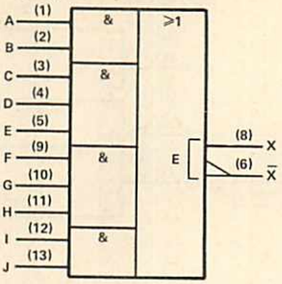
4-WIDE AND-OR EXPANDERS

typical performance

TYPE	POWER
'H62	25 mW

SN54H62 (J) SN74H62 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	A	8	X
2	B	9	F
3	C	10	G
4	D	11	H
5	E	12	I
6	$\overline{X}$	13	J
7	GND	14	V_{CC}

63

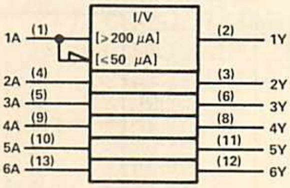
HEX CURRENT-SENSING INTERFACE GATES

typical performance

TYPE	POWER	DELAY
'LS63	3.3 mW	21 ns

SN54LS63 (J,FH) SN74LS63 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2Y	10	5A
4	2A	11	5Y
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2Y	14	5A
5	nc	15	nc
6	2A	16	5Y
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

64,65

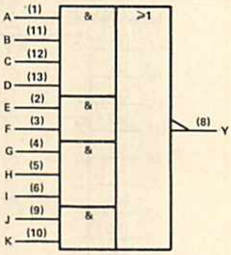
4-2-3-2 INPUT AND-OR-INVERT GATES

typical performance

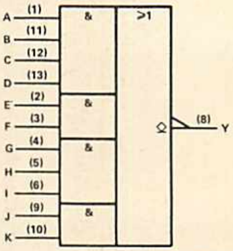
TYPE	OUTPUT	POWER	DELAY
'S64	TOTEM POLE	29 mW	3.5 ns
'S65	OPEN-COLLECTOR	36 mW	5.5 ns

SN54S64 (J,FH) SN74S64 (J,N,FN)
SN54S65 (J,FH) SN74S65 (J,N,FN)

logic symbol, 'S64†



logic symbol, 'S65†



positive logic: $Y = \overline{ABCD+EF+GHI+JK}$

pin assignments

J, N PACKAGES			
1	A	8	Y
2	E	9	J
3	F	10	K
4	G	11	B
5	H	12	C
6	I	13	D
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	A	12	Y
3	E	13	J
4	F	14	K
5	nc	15	nc
6	G	16	B
7	nc	17	nc
8	H	18	C
9	I	19	D
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

68

DUAL 4-BIT DECADE COUNTER

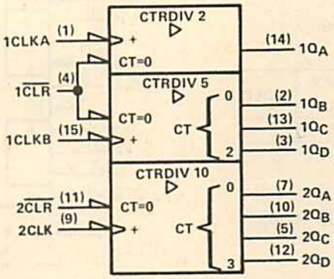
- High-drive outputs (I_{OL} rated at 8 mA/16 mA)

typical performance

COUNT FREQUENCY	CLEAR	POWER DISSIPATION
60 MHz	LOW	180 mW

SN54LS68 (J,FH) SN74LS68 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1CLKA	9	2CLK
2	$1Q_B$	10	$2Q_B$
3	$1Q_D$	11	$2\overline{CLR}$
4	$1\overline{CLR}$	12	$2Q_D$
5	$2Q_C$	13	$1Q_C$
6	nc	14	$1Q_A$
7	$2Q_A$	15	1CLKB
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1CLKA	12	2CLK
3	$1Q_B$	13	$2Q_B$
4	$1Q_D$	14	$2\overline{CLR}$
5	$1\overline{CLR}$	15	$2Q_D$
6	nc	16	nc
7	$2Q_C$	17	$1Q_C$
8	nc	18	$1Q_A$
9	$2Q_A$	19	1CLKB
10	GND	20	V_{CC}

nc – no internal connection

69

DUAL 4-BIT BINARY COUNTER

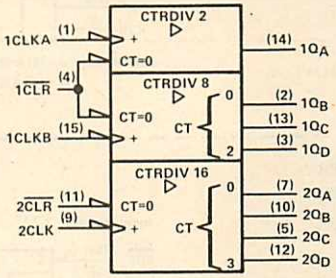
- High-drive outputs (I_{OL} rated at 8 mA/16 mA)

typical performance

COUNT FREQUENCY	CLEAR	POWER DISSIPATION
70 MHz	LOW	180 mW

SN54LS69 (J,FH) SN74LS69 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1CLKA	9	2CLK
2	$1Q_B$	10	$2Q_B$
3	$1Q_D$	11	$2\overline{CLR}$
4	$1\overline{CLR}$	12	$2Q_D$
5	$2Q_C$	13	$1Q_C$
6	nc	14	$1Q_A$
7	$2Q_A$	15	1CLKB
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1CLKA	12	2CLK
3	$1Q_B$	13	$2Q_B$
4	$1Q_D$	14	$2\overline{CLR}$
5	$1\overline{CLR}$	15	$2Q_D$
6	nc	16	nc
7	$2Q_C$	17	$1Q_C$
8	nc	18	$1Q_A$
9	$2Q_A$	19	1CLKB
10	GND	20	V_{CC}

nc – no internal connection

---

†Pin numbers shown on logic symbols are for J, JT and NT packages only.

nc – no internal connection.

70

AND-GATED J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

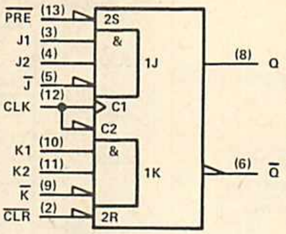
typical performance

TYPE	f_{max}	PWR/ FF	SET-UP	HOLD
'70	35 MHz	65 mW	20 ns↑	5 ns↑

↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN5470 (J,FH) SN7470 (J,N)

logic symbol†



positive logic: $J = J1 \cdot J2 \cdot \overline{J}$
$K = K1 \cdot K2 \cdot \overline{K}$
If inputs $\overline{J}$ and $\overline{K}$ are not used, they must be grounded.
Preset or clear function can occur only when the clock input is low.

pin assignments

J, N PACKAGES			
1	nc	8	Q
2	$\overline{CLR}$	9	$\overline{K}$
3	J1	10	K1
4	J2	11	K2
5	$\overline{J}$	12	CLK
6	$\overline{Q}$	13	$\overline{PRE}$
7	GND	14	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	nc	12	Q
3	$\overline{CLR}$	13	$\overline{K}$
4	J1	14	K1
5	nc	15	nc
6	J2	16	K2
7	nc	17	nc
8	$\overline{J}$	18	CLK
9	$\overline{Q}$	19	$\overline{PRE}$
10	GND	20	V_{CC}

71

'H71: AND-OR-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET

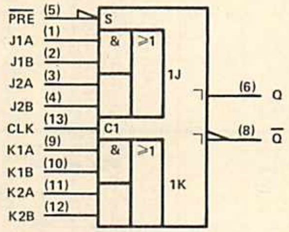
typical performance

TYPE	f_{max}	PWR/ FF	SET-UP	HOLD
'H71	30 MHz	80 mW	0 ns↑	0 ns↓
'L71	30 MHz	3.8 mW	0 ns↑	0 ns↓

↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN54H71 (J) SN74H71 (J,N)

logic symbol, 'H71†



positive logic: $J = (J1A \cdot J1B) + (J2A \cdot J2B)$
$K = (K1A \cdot K1B) + (K2A \cdot K2B)$

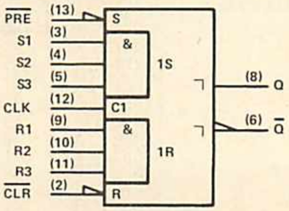
pin assignments, 'H71

J, N PACKAGES			
1	J1A	8	$\overline{Q}$
2	J1B	9	K1A
3	J2A	10	K1B
4	J2B	11	K2A
5	$\overline{PRE}$	12	K2B
6	Q	13	CLK
7	GND	14	V_{CC}

'L71: AND-GATED R-S MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

SN54L71 (J)

logic symbol, 'L71†



positive logic: $R = R1 \cdot R2 \cdot R3$
$S = S1 \cdot S2 \cdot S3$

pin assignments, 'L71

J, N PACKAGES			
1	nc	8	Q
2	$\overline{CLR}$	9	R1
3	S1	10	R2
4	S2	11	R3
5	S3	12	CLK
6	$\overline{Q}$	13	$\overline{PRE}$
7	GND	14	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

72

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

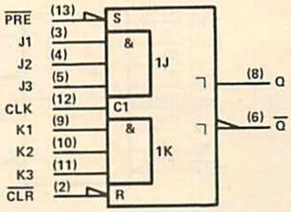
typical performance

TYPE	f_{max}	PWR/ FF	SET- UP	HOLD
'72	20 MHz	50 mW	0 ns↑	0 ns↓
'H72	30 MHz	80 mW	0 ns↑	0 ns↓
'L72	3 MHz	3.8 mW	0 ns↑	0 ns↓

↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN5472 (J,FH)	SN7472 (J)
SN54H72 (J)	SN74H72 (J)
SN54L72 (J)	

logic symbol†



positive logic: J = J1·J2·J3; K1·K2·K3

pin assignments

J, N PACKAGES			
1	nc	8	Q
2	$\overline{\text{CLR}}$	9	K1
3	J1	10	K2
4	J2	11	K3
5	J3	12	CLK
6	$\overline{\text{Q}}$	13	$\overline{\text{PRE}}$
7	GND	14	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	nc	12	Q
3	$\overline{\text{CLR}}$	13	K1
4	J1	14	K2
5	nc	15	nc
6	J2	16	K3
7	nc	17	nc
8	J3	18	CLK
9	$\overline{\text{Q}}$	19	$\overline{\text{PRE}}$
10	GND	20	V_{CC}

73

DUAL J-K FLIP-FLOPS WITH CLEAR

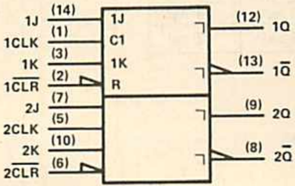
typical performance

TYPE	f_{max}	PWR/ F-F	SET- UP	HOLD
'73	20 MHz	5 mW	0 ns↑	0 ns↓
'H73	30 MHz	80 mW	0 ns↑	0 ns↓
'L73	3 MHz	3.8 mW	0 ns↑	0 ns↓
'LS73A	45 MHz	10 mW	20 ns↓	0 ns↓

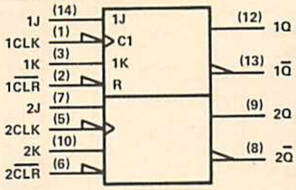
↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN5473 (J)	SN7473 (J,N)
SN54H73 (J)	SN74H73 (J,N)
SN54L73 (J)	
SN54LS73A (J	SN74LS73A (J,N)

logic symbol' '73, 'H73, 'L73†



logic symbol, 'LS73A†



pin assignments

J, N PACKAGES			
1	1CLK	8	2$\overline{\text{Q}}$
2	1$\overline{\text{CLR}}$	9	2Q
3	1K	10	2K
4	V_{CC}	11	GND
5	2CLK	12	1Q
6	2$\overline{\text{CLR}}$	13	1$\overline{\text{Q}}$
7	2J	14	1J

For chip carrier information, contact the factory.

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† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

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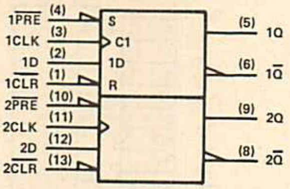
Product Guide

74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$1\overline{\text{CLR}}$	8	$2\overline{\text{Q}}$	1	nc	11	nc
2	1D	9	2Q	·2	$1\overline{\text{CLR}}$	12	$2\overline{\text{Q}}$
3	1CLK	10	$2\overline{\text{PRE}}$	3	1D	13	2Q
4	$1\overline{\text{PRE}}$	11	2CLK	4	1CLK	14	$2\overline{\text{PRE}}$
5	1Q	12	2D	5	nc	15	nc
6	$1\overline{\text{Q}}$	13	$2\overline{\text{CLR}}$	6	$1\overline{\text{PRE}}$	16	2CLK
7	GND	14	V_{CC}	7	nc	17	nc
				8	1Q	18	2D
				9	$1\overline{\text{Q}}$	19	$2\overline{\text{CLR}}$
				10	GND	20	V_{CC}

typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'74	25 MHz	43 mW	20 ns↑	5 ns↑
'ALS74	50 MHz	6 mW	15 ns↑	0 ns↑
'AS74	125 MHz	26 mW	4.5 ns↑	0 ns↑
'H74	43 MHz	75 mW	15 ns↑	5 ns↑
'L74	3 MHz	4 mW	50 ns↑	15 ns↑
'LS74A	33 MHz	10 mW	20 ns↑	5 ns↑
'S74	110 MHz	75 mW	3 ns↑	2 ns↑

↑ Rising edge of clock pulse.

SN5474 (J,FH)	SN7474 (J,N)
SN54ALS74 (J,FH)	SN74ALS74 (N,FN)
SN54AS74 (J,FH)	SN74AS74 (N,FN)
SN54H74 (J)	SN74H74 (J,N)
SN54L74 (J)	
SN54LS74A (J,FH)	SN74LS74A (J,N,FN)
SN54S74 (J,FH)	SN74S74 (J,N,FN)

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† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

75

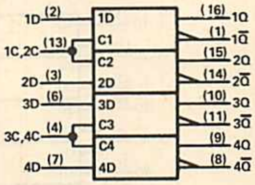
4-BIT BISTABLE LATCHES

typical performance

TYPE	OUT-PUTS	DELAY	TOTAL POWER
'75	Q,$\overline{Q}$	15 ns	160 mW
'L75	Q,$\overline{Q}$	30 ns	80 mW
'LS75	Q,$\overline{Q}$	11 ns	32 mW

SN5475 (J)	SN7475 (J,N)
SN54L75 (J)	
SN54LS75 (J)	SN74LS75 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1$\overline{Q}$	9	4Q
2	1D	10	3Q
3	2D	11	3$\overline{Q}$
4	3C,4C	12	GND
5	V_{CC}	13	1C,2C
6	3D	14	2$\overline{Q}$
7	4D	15	2Q
8	4$\overline{Q}$	16	1Q

For chip carrier information, contact the factory.

76

DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

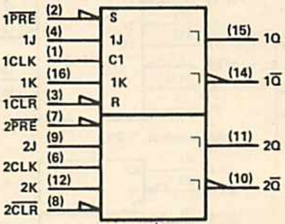
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'76	20 MHz	50 mW	0 ns↑	0 ns↓
'H76	30 MHz	80 mW	0 ns↑	0 ns↓
'LS76A	45 MHz	10 mW	20 ns↓	0 ns↓

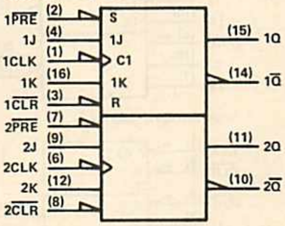
↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN5476 (J)	SN7476 (J,N)
SN54H76 (J)	SN74H76 (J,N)
SN54LS76A (J)	SN74LS76A (J,N)

logic symbol, '76, 'H76†



logic symbol, 'LS76A†



pin assignments

J, N PACKAGES			
1	1CLK	9	2J
2	1$\overline{PRE}$	10	2$\overline{Q}$
3	1$\overline{CLR}$	11	2Q
4	1J	12	2K
5	V_{CC}	13	GND
6	2CLK	14	1$\overline{Q}$
7	2$\overline{PRE}$	15	1Q
8	2$\overline{CLR}$	16	1K

For chip carrier information, contact the factory.

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

77

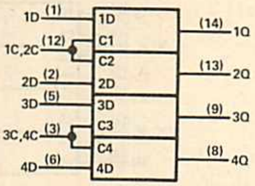
4-BIT BISTABLE LATCHES

typical performance

OUT-PUTS	DELAY	TOTAL POWER
Q	15 ns	160 mW
Q	30 ns	80 mW
Q	10 ns	35 mW

SN5477 (J)
SN54L77 (J)
SN54LS77 (J)

logic symbol†



pin assignments

J, N PACKAGES			
1	1D	8	4Q
2	2D	9	3Q
3	3C,4C	10	nc
4	V_{CC}	11	GND
5	3D	12	1C,2C
6	4D	13	2Q
7	nc	14	1Q

For chip carrier information, contact the factory.

78

DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

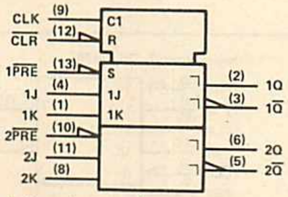
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'H78	30 MHz	80 mW	0 ns↑	0 ns↓
'L78	3 MHz	3.8 mW	0 ns↑	0 ns↓
'LS78A	45 MHz	10 mW	20 ns↓	0 ns↓

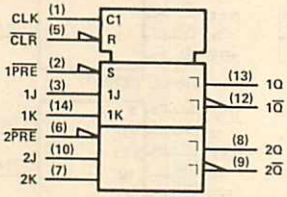
↑ Rising edge of clock pulse.
↓ Falling edge of clock pulse.

SN54H78 (J)	SN74H78 (J,N)
SN54L78 (J)	
SN54LS78A (J)	SN74LS78A (J,N)

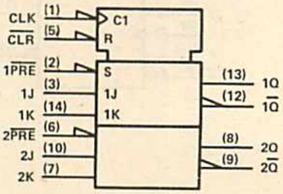
logic symbol, 'H78†



logic symbol, 'L78†



logic symbol, 'LS78A†



pin assignments, 'H78

J, N PACKAGES			
1	1K	8	2K
2	1Q	9	CLK
3	$1\overline{Q}$	10	$2\overline{PRE}$
4	1J	11	2J
5	$2\overline{Q}$	12	$\overline{CLR}$
6	2Q	13	$1\overline{PRE}$
7	GND	14	V_{CC}

pin assignments, 'L78, 'LS78A

J, N PACKAGES			
1	CLK	8	2Q
2	$1\overline{PRE}$	9	$2\overline{Q}$
3	1J	10	2J
4	V_{CC}	11	GND
5	$\overline{CLR}$	12	$1\overline{Q}$
6	$2\overline{PRE}$	13	1Q
7	2K	14	1K

For chip carrier information, contact the factory.

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† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

80

GATED FULL ADDERS

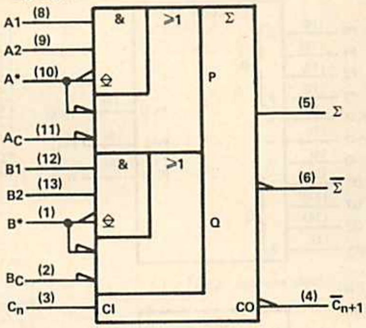
typical performance

TYPE	CARRY TIME	ADD TIME	POWER PER BIT
'80	10.5 ns	52 ns	105 mW

SN5480 (J,FH) SN7480 (J,N)

NOTES:
1. $A = \overline{A_C} + \overline{A^*} + A1 \cdot A2$, $B = \overline{B_C} + \overline{B^*} + B1 \cdot B2$
2. When A* is used as an input, A1 or A2 must be low. When B* is used as an input, B1 or B2 must be low.
3. When A1 and A2 or B1 and B2 are used as inputs, A* or B*, respectively, must be open or used to perform dot-AND logic.

logic symbol†



pin assignments

J, N PACKAGES			
1	B*	8	A1
2	B_C	9	A2
3	C_n	10	A*
4	$\overline{C}_{n+1}$	11	A_C
5	Σ	12	B1
6	$\overline{\Sigma}$	13	B2
7	GND	14	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	B*	12	A1
3	B_C	13	A2
4	C_n	14	A*
5	nc	15	nc
6	$\overline{C}_{n+1}$	16	A_C
7	nc	17	nc
8	Σ	18	B1
9	$\overline{\Sigma}$	19	B2
10	GND	20	V_{CC}

82

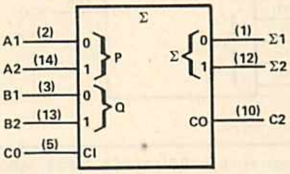
2-BIT BINARY FULL ADDERS

typical performance

TYPE	CARRY TIME	ADD TIME	POWER PER BIT
'82	14.5 ns	25 ns	87 mW

SN5482 (J) SN7482 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	Σ1	8	nc
2	A1	9	nc
3	B1	10	C2
4	V_{CC}	11	GND
5	CO	12	Σ2
6	nc	13	B2
7	nc	14	A2

For chip carrier information, contact the factory.

83

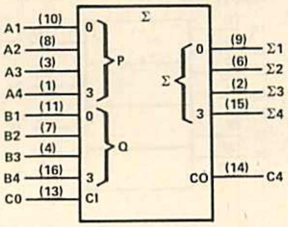
4-BIT BINARY FULL ADDERS WITH FAST CARRY

typical performance

TYPE	CARRY TIME	ADD TIME	POWER PER BIT
'83A	10 ns	16 ns	76 mW
'LS83A	10 ns	15 ns	24 mW

SN5483A (J) SN7483A (J,N)
SN54LS83A (J) SN74LS83A (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	A4	9	Σ1
2	ISI3	10	A1
3	A3	11	B1
4	B3	12	GND
5	V_{CC}	13	C0
6	Σ2	14	C4
7	B2	15	Σ4
8	A2	16	B4

For new chip carrier designs, use 'LS283 or 'S283.

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

85

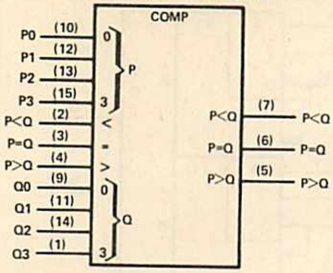
4-BIT MAGNITUDE COMPARATORS

typical performance

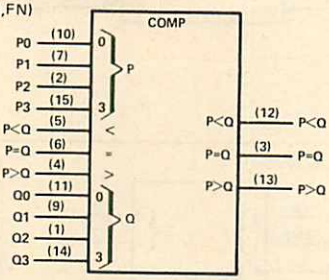
TYPE	COMPARE TIME	POWER
'85	21 ns	275 mW
'L85	82 ns	20 mW
'LS85	23.5 ns	52 mW
'S85	11.5 ns	365 mW

SN5485 (J,FH) SN7485 (J,N)
SN54L85 (J)
SN54LS85 (J,FH) SN74LS85 (J,N,FN)
SN54S85 (J,FH) SN74S85 (J,N,FN)

logic symbol, '85, 'LS85, 'S85†



logic symbol, 'L85†



pin assignments, '85, 'LS85, 'S85

J, N PACKAGES			
1	Q3	9	Q0
2	P<Qin	10	P0
3	P=Qin	11	Q1
4	P>Qin	12	P1
5	P>Qout	13	P2
6	P=Qout	14	Q2
7	P<Qout	15	P3
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	Q3	12	Q0
3	P<Qin	13	P0
4	P=Qin	14	Q1
5	P>Qin	15	P1
6	nc	16	nc
7	P>Qout	17	P2
8	P=Qout	18	Q2
9	P<Qout	19	P3
10	GND	20	V_{CC}

pin assignments, 'L85

J, N PACKAGES			
1	Q2	9	Q1
2	P2	10	P0
3	P=Qout	11	Q0
4	P>Qin	12	P<Qout
5	P<Qin	13	P>Qout
6	P=Qin	14	Q3
7	P1	15	P3
8	GND	16	V_{CC}

86

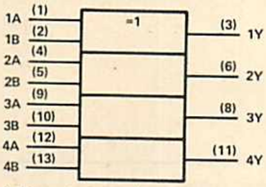
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

typical performance

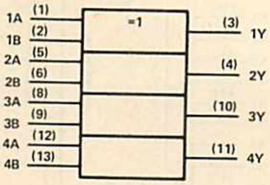
TYPE	POWER	DELAY
'86	150 mW	14 ns
'ALS86		
'L86	15 mW	55 ns
'LS86	30 mW	10 ns
'S86	250 mW	7 ns

SN5486 (J,FH) SN7486 (J,N)
SN54ALS86 (J,FH) SN74ALS86 (N,FN)
SN54L86 (J)
SN54LS86 (J,FH) SN74LS86 (J,N,FN)
SN54S86 (J,FH) SN74S86 (J,N,FN)

logic symbol, '86, 'ALS86, 'LS86, 'S86†



logic symbol, 'L86†



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

pin assignments, '86, 'ALS86, 'LS86, 'S86

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	nc	15	nc
6	2A	16	4Y
7	nc	17	nc
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

pin assignments, 'L86

J, N PACKAGES			
1	1A	8	3A
2	1B	9	3B
3	1Y	10	3Y
4	2Y	11	4Y
5	2A	12	4A
6	2B	13	4B
7	GND	14	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

87

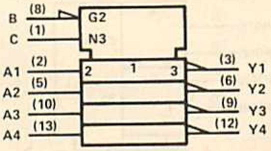
4-BIT TRUE/ COMPLEMENT, ZERO/ONE ELEMENTS

typical performance

TYPE	POWER	DELAY
'H87	270 mW	14 ns

SN54H87 (J) SN74H87 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	C	8	B
2	A1	9	Y3
3	Y1	10	A3
4	nc	11	nc
5	A2	12	Y4
6	Y2	13	A4
7	GND	14	V_{CC}

88

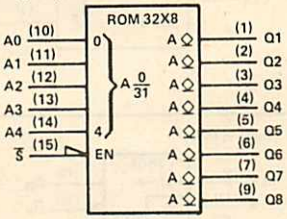
256-BIT READ-ONLY MEMORIES

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER PER BIT
'88A	26 ns	22 ns	1.1 mW

SN54488A (J) SN7488A (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	Q1	9	Q8
2	Q2	10	A0
3	Q3	11	A1
4	Q4	12	A2
5	Q5	13	A3
6	Q6	14	A4
7	Q7	15	$\overline{S}$
8	GND	16	V_{CC}

89

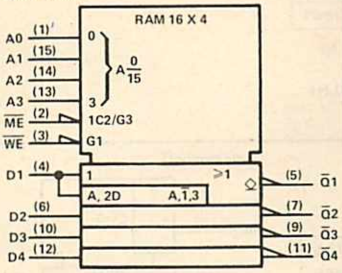
64-BIT READ/WRITE MEMORIES

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER PER BIT
'89	32 ns	30 ns	5.9 mW

SN7489 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	9	$\overline{Q}3$
2	$\overline{ME}$	10	D3
3	$\overline{WE}$	11	$\overline{Q}4$
4	D1	12	D4
5	$\overline{Q}1$	13	A3
6	D2	14	A2
7	$\overline{Q}2$	15	A1
8	GND	16	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

90

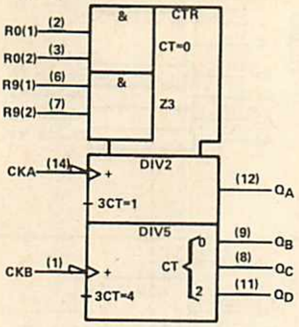
DECADE COUNTERS

typical performance

TYPE	COUNT FREQUENCY	CLEAR	TOTAL POWER
'90A	32 MHz	HIGH	160 mW
'L90	3 MHz	HIGH	20 mW
'LS90	32 MHz	HIGH	40 mW

SN5490A (J)	SN7490A (J,N)
SN54L90 (J)	
SN54LS90 (J)	SN74LS90 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	CKB	8	Q_C
2	R0(1)	9	Q_B
3	R0(2)	10	GND
4	nc	11	Q_D
5	V_{CC}	12	Q_A
6	R9(1)	13	nc
7	R9(2)	14	CKA

For new chip carrier designs, use '290 or 'LS290.

91

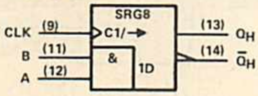
8-BIT SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQUENCY	SERIAL DATA INPUT	TOTAL POWER
'91A	10 MHz	GATED D	175 mW
'L91	3 MHz	GATED D	17.5 mW
'LS91	25 MHz	GATED D	60 mW

SN5491A (J)	SN7491A (J,N)
SN54L91 (J)	
SN54LS91 (J)	SN74LS91 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	nc	8	nc
2	nc	9	CLK
3	nc	10	GND
4	nc	11	B
5	V_{CC}	12	A
6	nc	13	QH
7	nc	14	QH

For chip carrier information, contact the factory.

92

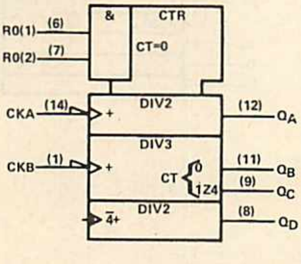
DIVIDE-BY-12 COUNTERS

typical performance

TYPE	COUNT FREQUENCY	CLEAR	TOTAL POWER
'92A	32 MHz	HIGH	160 mW
'LS92	32 MHz	HIGH	39 mW

SN5492A (J).	SN7492A (J,N)
SN54LS92 (J)	SN74LS92 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	CKB	8	Q_D
2	nc	9	Q_C
3	nc	10	GND
4	nc	11	Q_B
5	V_{CC}	12	Q_A
6	R0(1)	13	nc
7	R0(2)	14	CKA

For new chip carrier designs, use ''LS292.

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

93

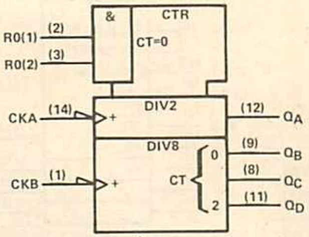
4-BIT BINARY COUNTERS

typical performance

TYPE	COUNT FREQUENCY	CLEAR	TOTAL POWER
'93A	32 MHz	HIGH	160 mW
'L93	3 MHz	HIGH	20 mW
'LS93	32 MHz	HIGH	39 mW

SN5493A (J)	SN7493A (J,N)
SN54L93 (J)	
SN54LS93 (J)	SN74LS93 (J,N)

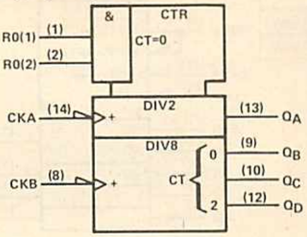
logic symbol, '93A, 'LS93†



pin assignments, '93A, 'LS93

J, N PACKAGES			
1	CKB	8	Q_C
2	R0(1)	9	Q_B
3	R0(2)	10	GND
4	nc	11	Q_D
5	V_{CC}	12	Q_A
6	nc	13	nc
7	nc	14	CKA

logic symbol, 'L93†



pin assignments, 'L93

J, N PACKAGES			
1	R0(1)	8	CKB
2	R0(2)	9	Q_B
3	nc	10	Q_C
4	V_{CC}	11	GND
5	nc	12	Q_D
6	nc	13	Q_A
7	nc	14	CKA

For new chip carrier designs, use '293 or 'LS293.

94

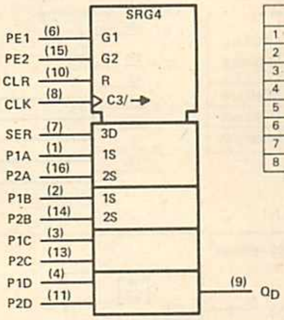
4-BIT SHIFT REGISTERS (DUAL ASYNCHRONOUS PRESETS)

typical performance

TYPE	SHIFT FREQUENCY	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'94	10 MHz	D	HIGH	175 mW

SN5494 (J)	SN7494 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	P1A	9	Q_D
2	P1B	10	CLR
3	P1C	11	P2D
4	P1D	12	GND
5	V_{CC}	13	P2C
6	PE1	14	P2B
7	SER	15	PE2
8	CLK	16	P2A

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

95

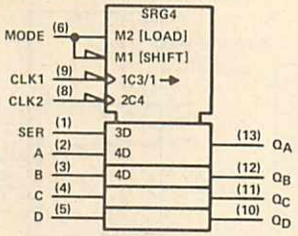
4-BIT SHIFT REGISTERS (PARALLEL IN/PARALLEL OUT, SHIFT RIGHT, SHIFT LEFT, SERIAL INPUT)

typical performance

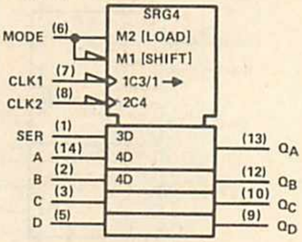
TYPE	SHIFT FREQUENCY	SERIAL DATA INPUT	TOTAL POWER
'95A	25 MHz	D	195 mW
'AS95			
'L95	3 MHz	D	19 mW
'LS95B	30 MHz	D	65 mW

SN5495A (J,FH) SN7495A (J,N)
SN54AS95 (J,FH) SN74AS95 (N,FN)
SN54L95 (J)
SN54LS95B (J,FH) SN74LS95B (J,N,FN)

logic symbol, '95A, 'AS95, 'LS95B†



logic symbol, 'L95†



pin assignments, '95A, 'LS95B

J, N PACKAGES			
1	SER	8	CLK2
2	A	9	CLK1
3	B	10	Q_D
4	C	11	Q_C
5	D	12	Q_B
6	MODE	13	Q_A
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	SER	12	CLK2
3	A	13	CLK1
4	B	14	Q_D
5	nc	15	nc
6	C	16	Q_C
7	nc	17	nc
8	D	18	Q_B
9	MODE	19	Q_A
10	GND	20	V_{CC}

pin assignments, 'L95

J, N PACKAGES			
1	SER	8	CLK2
2	B	9	Q_D
3	C	10	Q_C
4	V_{CC}	11	GND
5	D	12	Q_B
6	MODE	13	Q_A
7	CLK1	14	A

96

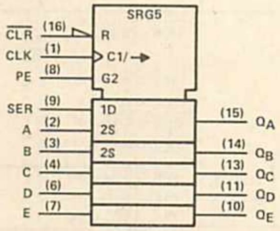
5-BIT SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQUENCY	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'96	10 MHz	D	LOW	240 mW
'L96	5 MHz	D	LOW	120 mW
'LS96	10 MHz	D	LOW	60 mW

SN5496 (J) SN7496 (J,N)
SN54L96 (J)
SN54LS96 (J) SN74LS96 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	CLK	9	SER
2	A	10	Q_E
3	B	11	Q_D
4	C	12	GND
5	V_{CC}	13	Q_C
6	D	14	Q_B
7	E	15	Q_A
8	PE	16	$\overline{CLR}$

For chip carrier information, contact the factory.

97

SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

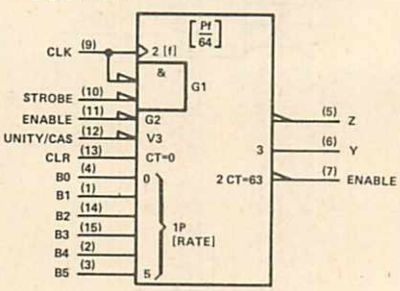
typical performance

TYPE	POWER	FREQ†
'97	345 mW	32 MHz

† Maximum clock frequency

SN5497 (J,FH)
SN7497 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	B1	9	CLK
2	B4	10	STRB
3	B5	11	ENin
4	B0	12	UNITY/CAS
5	Z	13	CLR
6	Y	14	B2
7	ENout	15	B3
8	GND	16	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	B1	12	CLK
3	B4	13	STRB
4	B5	14	ENin
5	B0	15	UNITY/CAS
6	nc	16	nc
7	Z	17	CLR
8	Y	18	B2
9	ENout	19	B3
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

98

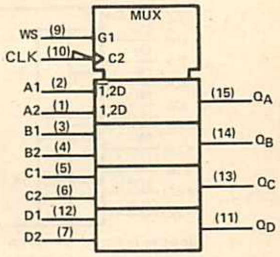
4-BIT DATA SELECTOR/ STORAGE REGISTERS

typical performance

TYPE	FREQUENCY	POWER
'L98	3 MHz	25 mW

SN54L98 (J)

logic symbol†



pin assignments

J, N PACKAGES			
1	A2	9	WS
2	A1	10	CLK
3	B1	11	Q_D
4	B2	12	D1
5	C1	13	Q_C
6	C2	14	Q_B
7	D2	15	Q_A
8	GND	16	V_{CC}

99

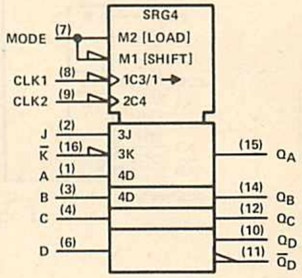
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQUENCY	SERIAL DATA INPUT	TOTAL POWER
'L99	3 MHz	J-$\overline{K}$	19 mW

SN54L99 (J)

logic symbol†



pin assignments

J, N PACKAGES			
1	A	9	CLK2
2	J	10	Q_D
3	B	11	$\overline{Q}_D$
4	C	12	Q_C
5	V_{CC}	13	GND
6	D	14	Q_B
7	MODE	15	Q_A
8	CLK1	16	$\overline{K}$

100

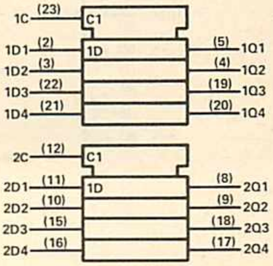
8-BIT BISTABLE LATCHES

typical performance

TYPE	DELAY	TOTAL POWER
'100	15 ns	320 mW

SN54100 (J) SN74100 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	nc	13	nc
2	1D1	14	nc
3	1D2	15	2D3
4	1Q2	16	2D4
5	1Q1	17	2Q4
6	nc	18	2Q3
7	GND	19	1Q3
8	2Q1	20	1Q4
9	2Q2	21	1D4
10	2D2	22	1D3
11	2D1	23	1C
12	2C	24	V_{CC}

For chip carrier information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

101

AND-OR-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

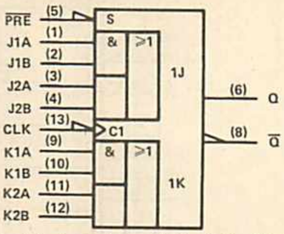
typical performance

TYPE	f_{max}	PWR	SET-UP	HOLD
'H101	50 MHz	100 mW	13 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54H101 (J) SN74H101 (J,N)

logic symbol†



positive logic: $J = (J1A \cdot J1B) + (J2A \cdot J2B)$
$K = (K1A \cdot K1B) + (K2A \cdot K2B)$

pin assignments

J, N PACKAGES			
1	J1A	8	$\overline{Q}$
2	J1B	9	K1A
3	J2A	10	K1B
4	J2B	11	K2A
5	$\overline{\text{PRE}}$	12	K2B
6	Q	13	CLK
7	GND	14	V_{CC}

102

AND-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

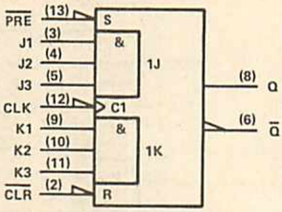
typical performance

TYPE	f_{max}	PWR	SET-UP	HOLD
'H102	50 MHz	100 mW	13 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54H102 (J) SN74H102 (J,N)

logic symbol†



positive logic: $J = J1 \cdot J2 \cdot J3$
$K = K1 \cdot K2 \cdot K3$

pin assignments

J, N PACKAGES			
1	nc	8	Q
2	$\overline{\text{CLR}}$	9	K1
3	J1	10	K2
4	J2	11	K3
5	J3	12	CLK
6	$\overline{Q}$	13	$\overline{\text{PRE}}$
7	GND	14	V_{CC}

103

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR

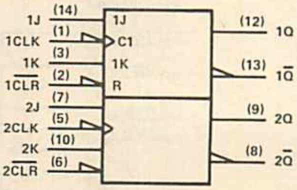
typical performance

TYPE	f_{max}	PWR/F-F	SET-UP	HOLD
'H103	50 MHz	100 mW	13 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54H103 (J) SN74H103 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1CLK	8	$\overline{\text{2Q}}$
2	$\overline{\text{1CLR}}$	9	2Q
3	1K	10	2K
4	V_{CC}	11	GND
5	2CLK	12	1Q
6	$\overline{\text{2CLR}}$	13	1Q
7	2J	14	1J

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

104

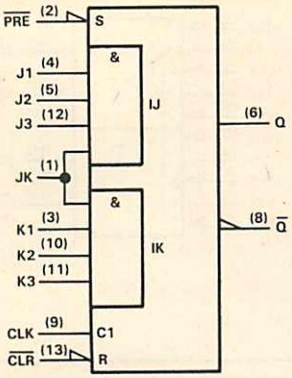
AND-GATED J-K MASTER-SLAVE FLIP-FLOPS

typical performance

TYPE	PWR	SET-UP	HOLD
'104	75 mW	10 ns↓	0 ns↓

SN54104 (J,FH) SN74104 (J,N)

logic symbol†



positive logic: J = J1•J2•J3
K = K1•K2•K3

pin assignments

J, N PACKAGE			
1	JK	8	$\overline{Q}$
2	$\overline{\text{PRE}}$	9	CLK
3	K1	10	K2
4	J1	11	K3
5	J2	12	J3
6	Q	13	$\overline{\text{CLR}}$
7	GND	14	V_{CC}

FH PACKAGE			
1	NC	11	NC
2	JK	12	$\overline{Q}$
3	$\overline{\text{PRE}}$	13	CLK
4	K1	14	K2
5	NC	15	NC
6	J1	16	K3
7	NC	17	NC
8	J2	18	J3
9	Q	19	$\overline{\text{CLR}}$
10	GND	20	V_{CC}

105

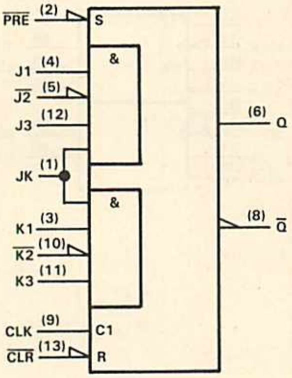
AND-GATED J-K MASTER-SLAVE FLIP-FLOPS

typical performance

TYPE	PWR	SET-UP	HOLD
'105	85 mW	10 ns↓	0 ns↓

SN54105 (J,FH) SN74105 (J,N)

logic symbol†



positive logic: J = J1•J2•J3
K = K1•K2•K3

pin assignments

J, N PACKAGE			
1	JK	8	$\overline{Q}$
2	$\overline{\text{PRE}}$	9	CLK
3	K1	10	$\overline{\text{K2}}$
4	J1	11	K3
5	$\overline{\text{J2}}$	12	J3
6	Q	13	$\overline{\text{CLR}}$
7	GND	14	V_{CC}

FH PACKAGE			
1	NC	11	NC
2	JK	12	Q
3	$\overline{\text{PRE}}$	13	CLK
4	K1	14	$\overline{\text{K2}}$
5	NC	15	NC
6	J1	16	K3
7	NC	17	NC
8	$\overline{\text{J2}}$	18	J2
9	Q	19	$\overline{\text{CLR}}$
10	GND	20	V_{CC}

---

†Pin numbers shown on logic symbols are for J and N packages only.

NC — no internal connection.

106

DUAL J-K NEGATIVE-EDGE TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

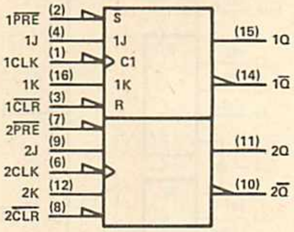
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'H106	50 MHz	100 mW	13 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54H106 (J) SN74H106 (J,N)

logic symbol†


1$\overline{\text{PRE}}$ (2)
1J (4)
1CLK (1)
1K (16)
1$\overline{\text{CLR}}$ (3)
2$\overline{\text{PRE}}$ (7)
2J (9)
2CLK (6)
2K (12)
2$\overline{\text{CLR}}$ (8)
S
1J
C1
1K
R
(15) 1Q
(14) 1$\overline{\text{Q}}$
(11) 2Q
(10) 2$\overline{\text{Q}}$

pin assignments

J, N PACKAGES			
1	1CLK	9	2J
2	1$\overline{\text{PRE}}$	10	2$\overline{\text{Q}}$
3	1$\overline{\text{CLR}}$	11	2Q
4	1J	12	2K
5	V_{CC}	13	GND
6	2CLK	14	1$\overline{\text{Q}}$
7	2$\overline{\text{PRE}}$	15	1Q
8	2$\overline{\text{CLR}}$	16	1K

107

DUAL J-K FLIP-FLOPS WITH CLEAR

typical performance

TYPE	f_{max}	PWR/ FF	SET-UP	HOLD
'107	20 MHz	50 mW	0 ns↑	0 ns↓
'LS107A	45 MHz	10 mW	20 ns↓	0 ns↓

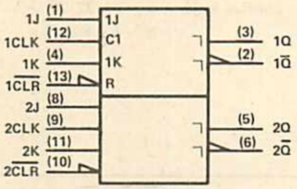
↑ Rising edge of clock pulse

↓ Falling edge of clock pulse

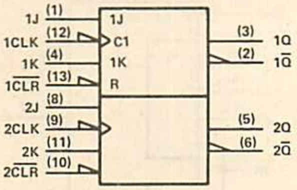
SN54107 (J,FH) SN74107 (J,N)

SN54LS107A (J,FH) SN74LS107A (J,N,FN)

logic symbol, '107†


1J (1)
1CLK (12)
1K (4)
1$\overline{\text{CLR}}$ (13)
2J (8)
2CLK (9)
2K (11)
2$\overline{\text{CLR}}$ (10)
1J
C1
1K
R
(3) 1Q
(2) 1$\overline{\text{Q}}$
(5) 2Q
(6) 2$\overline{\text{Q}}$

logic symbol, 'LS107A†


1J (1)
1CLK (12)
1K (4)
1$\overline{\text{CLR}}$ (13)
2J (8)
2CLK (9)
2K (11)
2$\overline{\text{CLR}}$ (10)
1J
C1
1K
R
(3) 1Q
(2) 1$\overline{\text{Q}}$
(5) 2Q
(6) 2$\overline{\text{Q}}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1J	8	2J	1	nc	11	nc
2	1$\overline{\text{Q}}$	9	2CLK	2	1J	12	2J
3	1Q	10	2$\overline{\text{CLR}}$	3	1$\overline{\text{Q}}$	13	2CLK
4	1K	11	2K	4	1Q	14	2$\overline{\text{CLR}}$
5	2Q	12	1CLK	5	nc	15	nc
6	2$\overline{\text{Q}}$	13	1$\overline{\text{CLR}}$	6	1K	16	2K
7	GND	14	V_{CC}	7	nc	17	nc
				8	2Q	18	1CLK
				9	2$\overline{\text{Q}}$	19	1$\overline{\text{CLR}}$
				10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

108

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

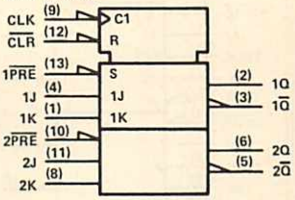
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'H108	50 MHz	100 mW	13 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54H108 (J) SN74H108 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1K	8	2K
2	1Q	9	CLK
3	$1\overline{Q}$	10	$2\overline{PRE}$
4	1J	11	2J
5	$2\overline{Q}$	12	$\overline{CLR}$
6	2Q	13	$1\overline{PRE}$
7	GND	14	V_{CC}

109

DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

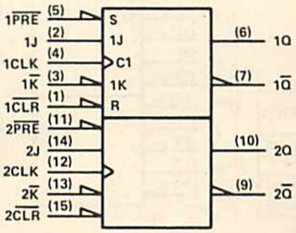
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'109	33 MHz	45 mW	10 ns↑	6 ns↑
'ALS109	50 MHz	6 mW	15 ns↑	0 ns↑
'AS109	125 MHz	29 mW	4.5 ns↑	0 ns↑
'LS109A	33 MHz	10 mW	20 ns↑	5 ns↑

↑ Rising edge of clock pulse

SN54109 (J,FH) SN74109 (J,N)
SN54ALS109 (J,FH) SN74ALS109 (N,FN)
SN54AS109 (J,FH) SN74AS109 (N,FN)
SN54LS109A (J,FH) SN74LS109A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$1\overline{CLR}$	9	$2\overline{Q}$
2	1J	10	2Q
3	$1\overline{K}$	11	$2\overline{PRE}$
4	1CLK	12	2CLK
5	$1\overline{PRE}$	13	$2\overline{K}$
6	1Q	14	2J
7	$1\overline{Q}$	15	$2\overline{CLR}$
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	$1\overline{CLR}$	12	$2\overline{Q}$
3	1J	13	2Q
4	$1\overline{K}$	14	$2\overline{PRE}$
5	1CLK	15	2CLK
6	nc	16	nc
7	$1\overline{PRE}$	17	$2\overline{K}$
8	1Q	18	2J
9	$1\overline{Q}$	19	$2\overline{CLR}$
10	GND	20	V_{CC}

110

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

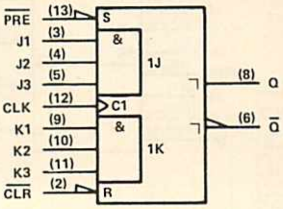
typical performance

TYPE	f_{max}	PWR	SET-UP	HOLD
'110	25 MHz	100 mW	20 ns↑	5 ns↑

↑ Rising edge of clock pulse

SN54110 (J) SN74110 (J,N)

logic symbol†



positive logic: J = J1 · J2 · J3
K = K1 · K2 · K3

pin assignments

J, N PACKAGES			
1	nc	8	Q
2	$\overline{CLR}$	9	K1
3	J1	10	K2
4	J2	11	K3
5	J3	12	CLK
6	$\overline{Q}$	13	$\overline{PRE}$
7	GND	14	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

111

DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

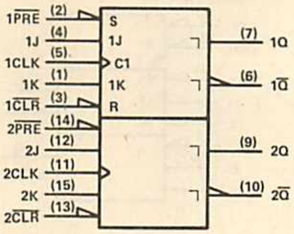
typical performance

TYPE	f_{max}	PWR/ FF	SET-UP	HOLD
'111	25 MHz	70 mW	0 ns↑	30 ns↑

↑ Rising edge of clock pulse

SN54111 (J) SN74111 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1K	9	2Q
2	$1\overline{PRE}$	10	$2\overline{Q}$
3	$1\overline{CLR}$	11	2CLK
4	1J	12	2J
5	1CLK	13	$2\overline{CLR}$
6	$1\overline{Q}$	14	$2\overline{PRE}$
7	1Q	15	2K
8	GND	16	V_{CC}

112

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

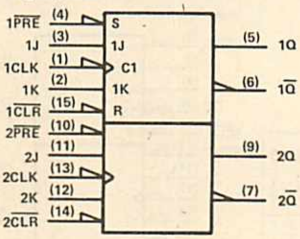
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'ALS112A	40 MHz	6 mW	25 ns↓	0 ns↓
'AS112	200 MHz	95 mW		
'LS112A	45 MHz	10 mW	20 ns↓	0 ns↓
'S112	125 MHz	75 mW	3 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54ALS112A (J,FH)	SN74ALS112A (N,FN)
SN54AS112 (J,FH)	SN74AS112 (N,FN)
SN54LS112A (J,FH)	SN74LS112A (J,N,FN)
SN54S112 (J,FH)	SN74S112 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1CLK	9	2Q	1	nc	11	nc
2	1K	10	$2\overline{PRE}$	2	1CLK	12	2Q
3	1J	11	2J	3	1K	13	$2\overline{PRE}$
4	$1\overline{PRE}$	12	2K	4	1J	14	2J
5	1Q	13	2CLK	5	$1\overline{PRE}$	15	2K
6	$1\overline{Q}$	14	$2\overline{CLR}$	6	nc	16	nc
7	$2\overline{Q}$	15	$1\overline{CLR}$	7	1Q	17	2CLK
8	GND	16	V_{CC}	8	$1\overline{Q}$	18	$2\overline{CLR}$
				9	$2\overline{Q}$	19	$1\overline{CLR}$
				10	GND	20	V_{CC}

113

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

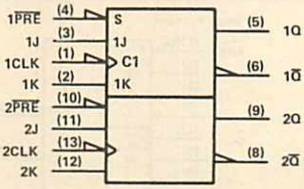
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'ALS113A	40 MHz	6 mW	25 ns↓	0 ns↓
'AS113	200 MHz	95 mW		
'LS113A	45 MHz	10 mW	20 ns↓	0 ns↓
'S113	125 MHz	75 mW	3 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54ALS113A (J,FH)	SN74ALS113A (N,FN)
SN54AS113 (J,FH)	SN74AS113 (N,FN)
SN54LS113A (J,FH)	SN74LS113A (J,N,FN)
SN54S113 (J,FH)	SN74S113 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1CLK	8	$2\overline{Q}$	1	nc	11	nc
2	1K	9	2Q	2	1CLK	12	$2\overline{Q}$
3	1J	10	$2\overline{PRE}$	3	1K	13	2Q
4	$1\overline{PRE}$	11	2J	4	1J	14	$2\overline{PRE}$
5	1Q	12	2K	5	nc	15	nc
6	$1\overline{Q}$	13	2CLK	6	$1\overline{PRE}$	16	2J
7	GND	14	V_{CC}	7	nc	17	nc
				8	1Q	18	2K
				9	$1\overline{Q}$	19	2CLK
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

114

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

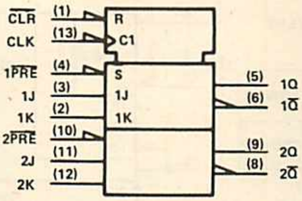
typical performance

TYPE	f_{max}	PWR/ F-F	SET-UP	HOLD
'ALS114A	40 MHz	6 mW	25 ns↓	0 ns↓
'AS114	200 MHz	95 mW		
'LS114A	45 MHz	10 mW	20 ns↓	0 ns↓
'S114	125 MHz	75 mW	3 ns↓	0 ns↓

↓ Falling edge of clock pulse

SN54ALS114A (J,FH)	SN74ALS114A (N,FN)
SN54AS114 (J,FH)	SN74AS114 (N,FN)
SN54LS114A (J,FH)	SN74LS114A (J,N,FN)
SN54S114 (J,FH)	SN74S114 (J,N,FN)

logic symbol[†]



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$1\overline{\text{CLR}}$	8	$2\overline{\text{Q}}$	1	nc	11	nc
2	1K	9	2Q	2	$1\overline{\text{CLR}}$	12	$2\overline{\text{Q}}$
3	1J	10	$2\overline{\text{PRE}}$	3	1K	13	2Q
4	$1\overline{\text{PRE}}$	11	2J	4	1J	14	$2\overline{\text{PRE}}$
5	1Q	12	2K	5	nc	15	nc
6	$1\overline{\text{Q}}$	13	CLK	6	$1\overline{\text{PRE}}$	16	2J
7	GND	14	V_{CC}	7	nc	17	nc
				8	1Q	18	2K
				9	$1\overline{\text{Q}}$	19	CLK
				10	GND	20	V_{CC}

116

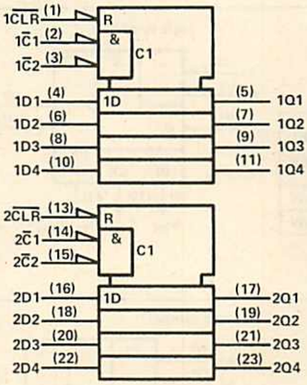
DUAL 4-BIT LATCHES

typical performance

TYPE	BITS	CLEAR	DELAY	TOTAL POWER
'116	8	LOW	11 ns	250 mW

SN54116 (J,FH)	SN74116 (J,N)

logic symbol[†]



pin assignments

J, N PACKAGES				FH PACKAGE			
1	$1\overline{\text{CLR}}$	13	$2\overline{\text{CLR}}$	1	nc	15	nc
2	$1\overline{\text{C}}1$	14	$2\overline{\text{C}}1$	2	$1\overline{\text{CLR}}$	16	$2\overline{\text{CLR}}$
3	$1\overline{\text{C}}2$	15	$2\overline{\text{C}}2$	3	$1\overline{\text{C}}1$	17	$2\overline{\text{C}}1$
4	1D1	16	2D1	4	$1\overline{\text{C}}2$	18	$2\overline{\text{C}}2$
5	1Q1	17	2Q1	5	1D1	19	2D1
6	1D2	18	2D2	6	1Q1	20	2Q1
7	1Q2	19	2Q2	7	1D2	21	2D2
8	1D3	20	2D3	8	nc	22	nc
9	1Q3	21	2Q3	9	1Q2	23	2Q2
10	1D4	22	2D4	10	1D3	24	2D3
11	1Q4	23	2Q4	11	1Q3	25	2Q3
12	GND	24	V_{CC}	12	1D4	26	2D4
				13	1Q4	27	2Q4
				14	GND	28	V_{CC}

[†] Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

120

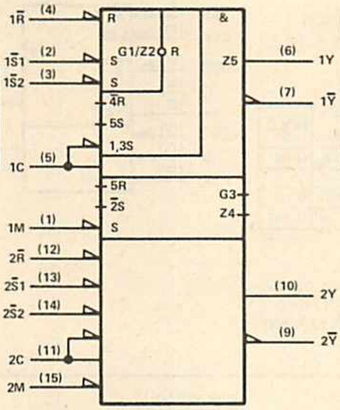
DUAL PULSE SYNCHRONIZERS/DRIVERS

typical performance

TYPE	ENABLE INPUT	COMP OUTPUT	FREQ RANGE	POWER
'120	YES	YES	DC to 30 MHz	255 mW

SN54120 (J,FH) SN74120 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1M	9	$2\overline{Y}$
2	$1\overline{S}1$	10	2Y
3	$1\overline{S}2$	11	2C
4	1R	12	$2\overline{R}$
5	1C	13	$2\overline{S}1$
6	1Y	14	$2\overline{S}2$
7	$1\overline{Y}$	15	2M
8	GND	16	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	1M	12	$2\overline{Y}$
3	$1\overline{S}1$	13	2Y
4	$1\overline{S}2$	14	2C
5	$1\overline{R}$	15	$2\overline{R}$
6	nc	16	nc
7	1C	17	$2\overline{S}1$
8	$1\overline{Y}$	18	$2\overline{S}2$
9	1Y	19	2M
10	GND	20	V_{CC}

121

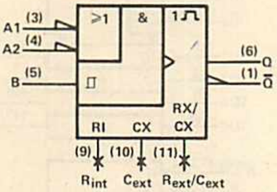
MONOSTABLE MULTIVIBRATORS

typical performance

TYPE	NO. OF INPUTS		OUTPUT PULSE RANGE	TOTAL POWER
	HI	LO		
'121	1	2	40 ns-28 s	90 mW
'L121	1	2	40 ns-28 s	40 mW

SN54121 (J) SN74121 (J,N)
SN54L121 (J)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{Q}$	8	nc
2	nc	9	R_{int}
3	A1	10	C_{ext}
4	A2	11	R_{ext}/C_{ext}
5	B	12	nc
6	Q	13	nc
7	GND	14	V_{CC}

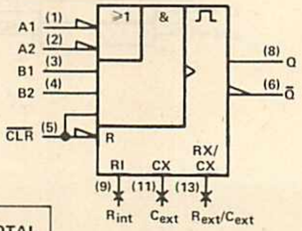
'121 . . . R_{int} = 2 kΩ nominal
'L121 . . . R_{int} = 4 kΩ nominal

122

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

- Up to 100% duty cycle
- Will not trigger from clear

logic symbol†



pin assignments

J, N PACKAGES			
1	A1	8	Q
2	A2	9	R_{INT}
3	B1	10	nc
4	B2	11	C_{EXT}
5	$\overline{CLR}$	12	nc
6	$\overline{Q}$	13	R_{ext}/C_{ext}
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	A1	12	Q
3	A2	13	R_{int}
4	B1	14	nc
5	nc	15	nc
6	B2	16	C_{ext}
7	nc	17	nc
8	$\overline{CLR}$	18	nc
9	$\overline{Q}$	19	R_{ext}/C_{ext}
10	GND	20	V_{CC}

typical performance

TYPE	NO. OF INPUTS		DIRECT CLEAR	OUTPUT PULSE RANGE	TOTAL POWER
	HI	LO			
'122	2	2	YES	45 ns-∞	115 mW
'L122	2	2	YES	90 ns-∞	55 mW
'LS122	2	2	YES	45 ns-∞	30 mW

SN54122 (J,FH) SN74122 (J,N)
SN54L122 (J)
SN54LS122 (J,FH) SN74LS122 (J,N,FN)

'122 . . . R_{int} = 10 kΩ nominal
'L122 . . . R_{int} = 20 kΩ nominal
'LS122 . . . R_{int} = 10 kΩ nominal

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† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

123

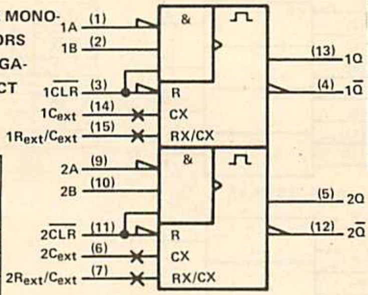
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH POSITIVE AND NEGATIVE INPUTS AND DIRECT CLEAR

typical performance

TYPE	OUTPUT PULSE RANGE	TOTAL POWER
'123	45 ns-∞	230 mW
'L123	90 ns-∞	115 mW
'LS123	45 ns-∞	60 mW

SN54123 (J,FH) SN74123 (J,N)
SN54L123 (J)
SN54LS123 (J,FH) SN74LS123 (J,N,FN)

logic symbol†


1A (1)
1B (2)
1$\overline{\text{CLR}}$ (3)
1C_{ext} (14)
1R_{ext}/C_{ext} (15)
&
R
CX
RX/CX
(13) 1Q
(4) 1$\overline{\text{Q}}$
2A (9)
2B (10)
2$\overline{\text{CLR}}$ (11)
2C_{ext} (6)
2R_{ext}/C_{ext} (7)
&
R
CX
RX/CX
(5) 2Q
(12) 2$\overline{\text{Q}}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	9	2A	1	nc	11	nc
2	1B	10	2B	2	1A	12	2A
3	1$\overline{\text{CLR}}$	11	2$\overline{\text{CLR}}$	3	1B	13	2B
4	1$\overline{\text{Q}}$	12	2$\overline{\text{Q}}$	4	1$\overline{\text{CLR}}$	14	2$\overline{\text{CLR}}$
5	2Q	13	1Q	5	1$\overline{\text{Q}}$	15	2$\overline{\text{Q}}$
6	2C_{ext}	14	1C_{ext}	6	nc	16	nc
7	2R_{ext}/C_{ext}	15	1R_{ext}/C_{ext}	7	2Q	17	1Q
8	GND	16	V_{CC}	8	2C_{ext}	18	1C_{ext}
				9	2R_{ext}/C_{ext}	19	1R_{ext}/C_{ext}
				10	GND	20	V_{CC}

124

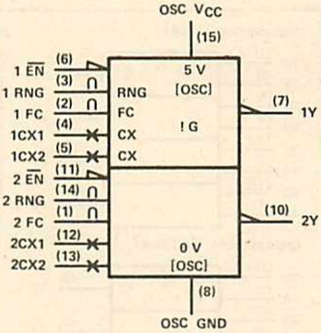
DUAL VOLTAGE-CONTROLLED OSCILLATORS WITH ENABLE INPUTS

typical performance

TYPE	FREQ RANGE	POWER
'S124	1 Hz to 60 MHz	525 mW

SN54S124 (J,FH) SN74S124 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	2FC	9	GND	1	nc	11	nc
2	1FC	10	2Y	2	2FC	12	GND
3	1RNG	11	2$\overline{\text{EN}}$	3	1FC	13	2Y
4	1CX1	12	2CX1	4	1RNG	14	2$\overline{\text{EN}}$
5	1CX2	13	2CX2	5	1CX1	15	2CX1
6	1$\overline{\text{EN}}$	14	2RNG	6	nc	16	nc
7	1Y	15	OSC V_{CC}	7	1CX2	17	2CX2
8	OSC GND	16	V_{CC}	8	1$\overline{\text{EN}}$	18	2RNG
				9	1Y	19	OSC V_{CC}
				10	OSC GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

125

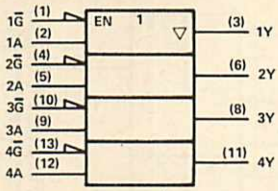
QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

typical performance

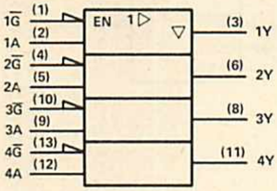
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54125	10 ns	−2 mA	16 mA
SN74125	10 ns	−5.2 mA	16 mA
SN54LS125A	8 ns	−1 mA	12 mA
SN74LS125A	8 ns	−2.6 mA	24 mA

SN54125 (J,FH) SN74125 (J,N)
SN54LS125A (J,FH) SN74LS125A (J,N,FN)

logic symbol, '125†



logic symbol, 'LS125A†



positive logic: Y = A

pin assignments

J, N PACKAGES			
1	$1\overline{G}$	8	3Y
2	1A	9	3A
3	1Y	10	$3\overline{G}$
4	$2\overline{G}$	11	4Y
5	2A	12	4A
6	2Y	13	$4\overline{G}$
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	$1\overline{G}$	12	3Y
3	1A	13	3A
4	1Y	14	$3\overline{G}$
5	nc	15	nc
6	$2\overline{G}$	16	4Y
7	nc	17	nc
8	2A	18	4A
9	2Y	19	$4\overline{G}$
10	GND	20	V_{CC}

126

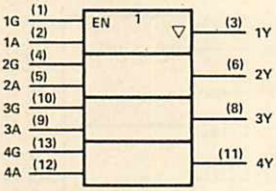
QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

typical performance

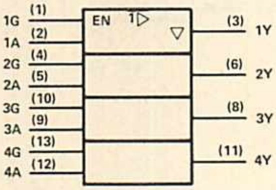
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54126	10 ns	−2 mA	16 mA
SN74126	10 ns	−5.2 mA	16 mA
SN54LS126A	8.5 ns	−1 mA	12 mA
SN74LS126A	8.5 ns	−2.6 mA	24 mA

SN54126 (J,FH) SN74126 (J,N)
SN54LS126A (J,FH) SN74LS126A (J,N,FN)

logic symbol, '126†



logic symbol, 'LS126A†



positive logic: Y = A

pin assignments

J, N PACKAGES			
1	1G	8	3Y
2	1A	9	3A
3	1Y	10	3G
4	2G	11	4Y
5	2A	12	4A
6	2Y	13	4G
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1G	12	3Y
3	1A	13	3A
4	1Y	14	3G
5	nc	15	nc
6	2G	16	4Y
7	nc	17	nc
8	2A	18	4A
9	2Y	19	4G
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

128

LINE DRIVERS

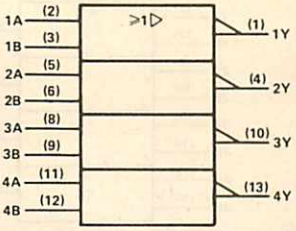
(SN54128 . . . 75 Ω DRIVER
SN74128 . . . 50 Ω DRIVER)

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY
SN54128	48 mA	−29 mA	7 ns
SN74128	48 mA	−42.4 mA	7 ns

SN54128 (J,FH) SN74128 (J,N)

logic symbol†



positive logic: Y = $\overline{A+B}$

pin assignments

J, N PACKAGES			
1	1Y	8	3A
2	1A	9	3B
3	1B	10	3Y
4	2Y	11	4A
5	2A	12	4B
6	2B	13	4Y
7	GND	14	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	1Y	12	3A
3	1A	13	3B
4	1B	14	3Y
5	nc	15	nc
6	2Y	16	4A
7	nc	17	nc
8	2A	18	4B
9	2B	19	4Y
10	GND	20	V_{CC}

131

3- TO 8-LINE DECODERS/ DEMULTIPLEXERS WITH ADDRESS REGISTERS

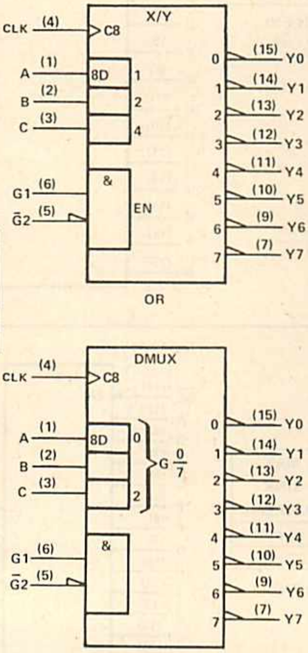
(combines decoder and 3-bit address register and incorporates 2 enable inputs to simplify cascading)

typical performance

TYPE	CLOCK TO OUTPUT	ENABLE TIME	TOTAL POWER
'ALS131	8.5 ns	10 ns	25 mW
'AS131			

SN54ALS131 (J,FH) SN74ALS131 (N,FN)
SN54AS131 (J,FH) SN74AS131 (N,FN)

logic symbols†



pin assignments

J, N PACKAGES			
1	A	9	Y6
2	B	10	Y5
3	C	11	Y4
4	CLK	12	Y3
5	$\overline{G}2$	13	Y2
6	G1	14	Y1
7	Y7	15	Y0
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	A	12	Y6
3	B	13	Y5
4	C	14	Y4
5	CLK	15	Y3
6	nc	16	nc
7	$\overline{G}2$	17	Y2
8	G1	18	Y1
9	Y7	19	Y0
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

132

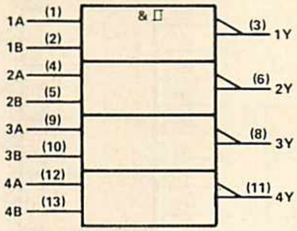
QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

typical performance

TYPE	HYSTERESIS	DELAY
'132	0.8 V	15 ns
'LS132	0.8 V	15 ns
'S132	0.55 V	8 ns

SN54132 (J,FH) SN74132 (J,N)
SN54LS132 (J,FH) SN74LS132 (J,N,FN)
SN54S132 (J,FH) SN74S132 (J,N,FN)

logic symbol†



positive logic: Y = $\overline{AB}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3Y	1	nc	11	nc
2	1B	9	3A	2	1A	12	3Y
3	1Y	10	3B	3	1B	13	3A
4	2A	11	4Y	4	1Y	14	3B
5	2B	12	4A	5	nc	15	nc
6	2Y	13	4B	6	2A	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2B	18	4A
				9	2Y	19	4B
				10	GND	20	V_{CC}

133

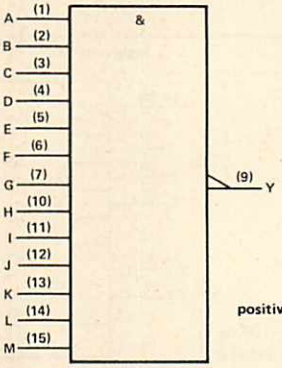
13-INPUT POSITIVE-NAND GATES

typical performance

TYPE	POWER	DELAY
'ALS133	2 mW	8 ns
'S133	19 mW	3 ns

SN54ALS133 (J,FH) SN74ALS133 (N,FN)
SN54S133 (J,FH) SN74S133 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A	9	Y	1	nc	11	nc
2	B	10	H	2	A	12	Y
3	C	11	I	3	B	13	H
4	D	12	J	4	C	14	I
5	E	13	K	5	D	15	J
6	F	14	L	6	nc	16	nc
7	G	15	M	7	E	17	K
8	GND	16	V_{CC}	8	F	18	L
				9	G	19	M
				10	GND	20	V_{CC}

positive logic: Y = $\overline{ABCDEFGHIJKLM}$

134

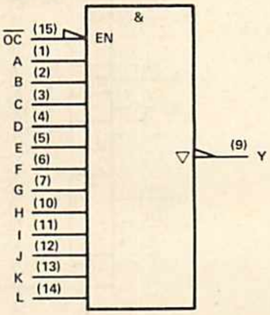
12-INPUT POSITIVE-NAND GATES WITH THREE-STATE OUTPUTS

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54S134	4.5 ns	−2 mA	20 mA
SN74S134	4.5 ns	−6.5 mA	20 mA

SN54S134 (J,FH) SN74S134 (J,N,FN)

logic symbol†



positive logic: Y = $\overline{ABCDEFGHIJKL}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A	9	Y	1	nc	11	nc
2	B	10	H	2	A	12	Y
3	C	11	I	3	B	13	H
4	D	12	J	4	C	14	I
5	E	13	K	5	D	15	J
6	F	14	L	6	nc	16	nc
7	G	15	$\overline{OC}$	7	E	17	K
8	GND	16	V_{CC}	8	F	18	L
				9	G	19	$\overline{OC}$
				10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

135

QUAD EXCLUSIVE OR/NOR GATES

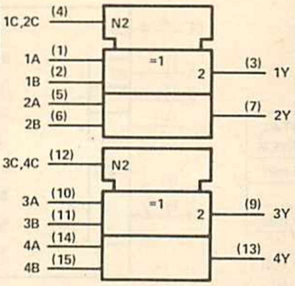
SN54S135 (J,FH)

typical performance

TYPE	POWER	DELAY
'S135	325 mW	8 ns

SN74S135 (J,N,FN)

logic symbol†



positive logic: $Y = A \oplus B \oplus C = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$

pin assignments

J, N PACKAGES			
1	1A	9	3Y
2	1B	10	3A
3	1Y	11	3B
4	1C,2C	12	3C,4C
5	2A	13	4Y
6	2B	14	4A
7	2Y	15	4B
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	1C,2C	15	3C,4C
6	nc	16	nc
7	2A	17	4Y
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

136

QUAD EXCLUSIVE-OR GATES WITH OPEN-COLLECTOR OUTPUTS

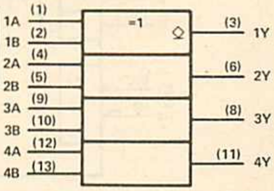
SN54136 (J,FH)
SN54LS136 (J,FH)

typical performance

TYPE	POWER	DELAY
'136	150 mW	27 ns
'LS136	30 mW	18 ns

SN74136 (J,N)
SN74LS136 (J,N,FN)

logic symbol†



positive logic: $Y = A \oplus B = A\bar{B} + \bar{A}B$

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	nc	15	nc
6	2A	16	4Y
7	nc	17	nc
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

137

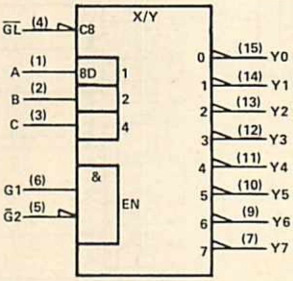
3- TO 8-LINE DECODERS/ DEMULTIPLEXERS WITH ADDRESS LATCHES

typical performance

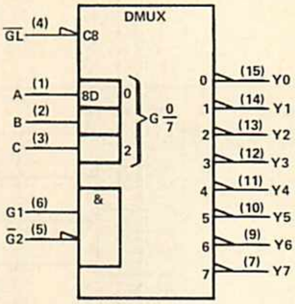
TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'ALS137	11 ns	10 ns	25 mW
'AS137			
'LS137	17.5 ns	16 ns	55 mW

SN54ALS137 (J,FH)	SN74ALS137 (N,FN)
SN54AS137 (J,FH)	SN74AS137 (N,FN)
SN54LS137 (J,FH)	SN74LS137 (J,N,FN)

logic symbol†



OR



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A	9	Y6	1	nc	11	nc
2	B	10	Y5	2	A	12	Y6
3	C	11	Y4	3	B	13	Y5
4	$\overline{GL}$	12	Y3	4	C	14	Y4
5	$\overline{G2}$	13	Y2	5	$\overline{GL}$	15	Y3
6	G1	14	Y1	6	nc	16	nc
7	Y7	15	Y0	7	$\overline{G2}$	17	Y2
8	GND	16	V_{CC}	8	G1	18	Y1
				9	Y7	19	Y0
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

138

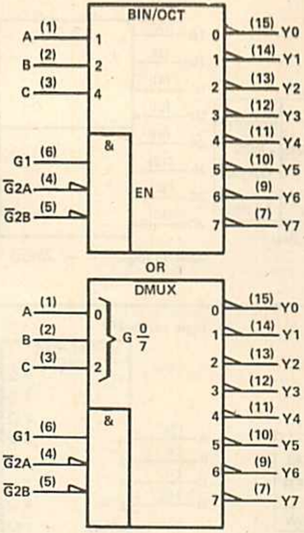
3- TO 8-LINE DECODERS/ DEMULTIPLEXERS

typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'ALS138	8.5 ns	9 ns	25 mW
'AS138			
'LS138	22 ns	21 ns	31 mW
'S138	8 ns	7 ns	245 mW

SN54ALS138 (J,FH)	SN74ALS138 (N,FN)
SN54AS138 (J,FH)	SN74AS138 (N,FN)
SN54LS138 (J,FH)	SN74LS138 (J,N,FN)
SN54S138 (J,FH)	SN74S138 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	A	9	Y6
2	B	10	Y5
3	C	11	Y4
4	$\overline{G}$2A	12	Y3
5	$\overline{G}$2B	13	Y2
6	G1	14	Y1
7	Y7	15	Y0
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	A	12	Y6
3	B	13	Y5
4	C	14	Y4
5	$\overline{G}$2A	15	Y3
6	nc	16	nc
7	$\overline{G}$2B	17	Y2
8	G1	18	Y1
9	Y7	19	Y0
10	GND	20	V_{CC}

139

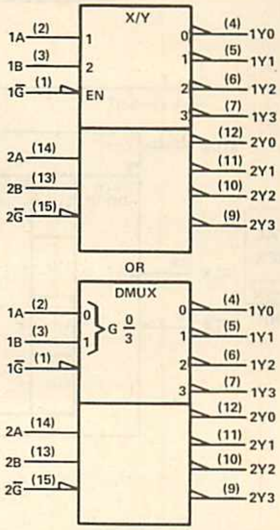
DUAL 2- TO 4-LINE DECODERS/DEMULTIPLEXERS

typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'ALS139			
'AS139			
'LS139	22 ns	19 ns	34 mW
'S139	7.5 ns	6 ns	300 mW

SN54ALS139 (J,FH)	SN74ALS139 (N,FN)
SN54AS139 (J,FH)	SN74AS139 (N,FN)
SN54LS139 (J,FH)	SN74LS139 (J,N,FN)
SN54S139 (J,FH)	SN74S139 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1$\overline{G}$	9	2Y3
2	1A	10	2Y2
3	1B	11	2Y1
4	1Y0	12	2Y0
5	1Y1	13	2B
6	1Y2	14	2A
7	1Y3	15	2$\overline{G}$
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1$\overline{G}$	12	2Y3
3	1A	13	2Y2
4	1B	14	2Y1
5	1Y0	15	2Y0
6	nc	16	nc
7	1Y1	17	2B
8	1Y2	18	2A
9	1Y3	19	2$\overline{G}$
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

140

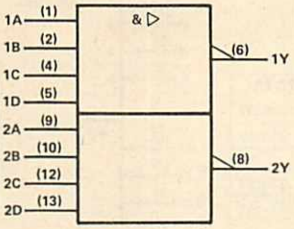
DUAL 4-INPUT POSITIVE-NAND 50-OHM LINE DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER PER GATE
'S140	60 mA	–40 mA	4 ns	44 mW

SN54S140 (J,FH) SN74S140 (J,N,FN)

logic symbol†



positive logic: Y = $\overline{ABCD}$

pin assignments

J, N PACKAGES			
1	1A	8	2Y
2	1B	9	2A
3	nc	10	2B
4	1C	11	nc
5	1D	12	2C
6	1Y	13	2D
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	2Y
3	1B	13	2A
4	nc	14	2B
5	nc	15	nc
6	1C	16	nc
7	nc	17	nc
8	1D	18	2C
9	1Y	19	2D
10	GND	20	V_{CC}

141

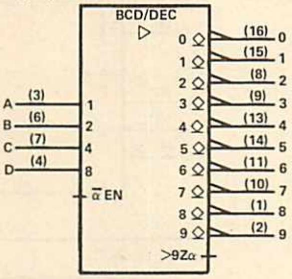
BCD-TO-DECIMAL DECODER/DRIVER

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'141	7 mA	60 V	80 mW

SN74141 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	8	9	3
2	9	10	7
3	A	11	6
4	D	12	GND
5	V_{CC}	13	4
6	B	14	5
7	C	15	1
8	2	16	0

142

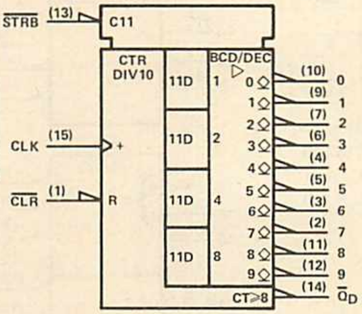
COUNTER/LATCH/ DECODER/DRIVER

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'142	7 mA	55 V	340 mW

SN74142 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{\text{CLR}}$	9	1
2	7	10	0
3	6	11	8
4	4	12	9
5	5	13	$\overline{\text{STRB}}$
6	3	14	$\overline{Q_D}$
7	2	15	CLK
8	GND	16	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

143,144

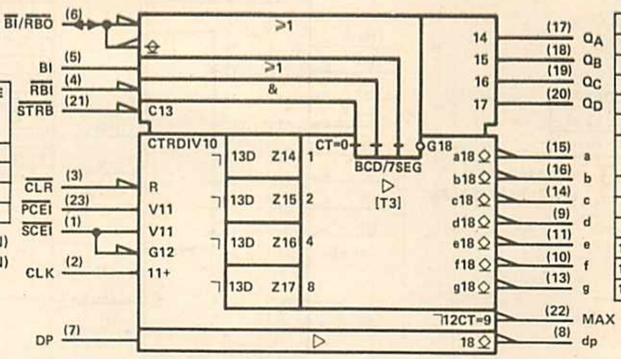
COUNTERS/LATCHES/ DECODERS/DRIVERS

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE
SN54143	15 mA*	7 V
SN74143	15 mA*	7 V
SN54144	20 mA	15 V
SN74144	25 mA	15 V

SN54143 (J) SN74143 (J,N)
SN54144 (J) SN74144 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{SCEI}$	13	g
2	CLK	14	c
3	$\overline{CLR}$	15	a
4	$\overline{RBI}$	16	b
5	BI	17	QA
6	$\overline{BI}/\overline{RBO}$	18	AB
7	DP	19	QC
8	dp	20	QD
9	d	21	$\overline{STRB}$
10	f	22	MAX
11	e	23	$\overline{PCEI}$
12	GND	24	V_{CC}

145

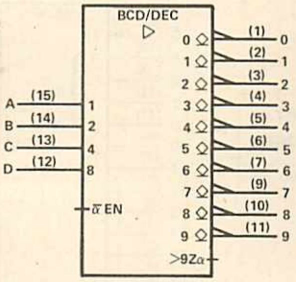
BCD-TO-DECIMAL DECODERS/ DRIVERS FOR LAMPS, RELAYS, MOS

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'145	80 mA	15 V	215 mW
'54LS145	12 mA	15 V	35 mW
'74LS145	80 mA	15 V	35 mW

SN54145 (J,FH) SN74145 (J,N)
SN54LS145 (J,FH) SN74LS145 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	0	9	7	1	nc	11	nc
2	1	10	8	2	0	12	7
3	2	11	9	3	1	13	8
4	3	12	D	4	2	14	9
5	4	13	C	5	3	15	D
6	5	14	B	6	nc	16	nc
7	6	15	A	7	4	17	C
8	GND	16	V_{CC}	8	5	18	B
				9	6	19	A
				10	GND	20	V_{CC}

147

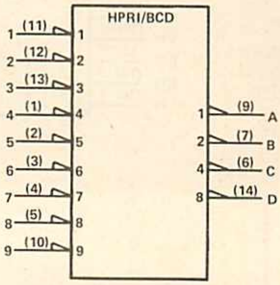
10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODERS

typical performance

TYPE	POWER	DELAY
'147	225 mW	10 ns
'LS147	60 mW	15 ns

SN54147 (J,FH) SN74147 (J,N)
SN54LS147 (J,FH) SN74LS147 (J,N,FN)

logic symbol†

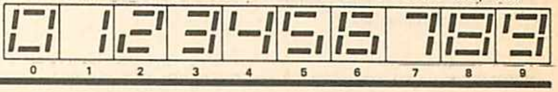


pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	4	9	A	1	nc	11	nc
2	5	10	9	2	4	12	A
3	6	11	1	3	5	13	9
4	7	12	2	4	6	14	1
5	8	13	3	5	7	15	2
6	C	14	D	6	nc	16	nc
7	B	15	nc	7	8	17	3
8	GND	16	V_{CC}	8	C	18	D
				9	B	19	nc
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

FONT TABLE T3 – RESULTANT DISPLAYS USING '143, '144



148

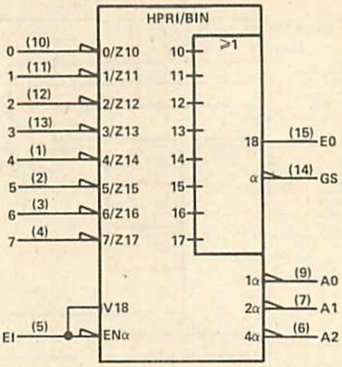
8- TO 3-LINE OCTAL PRIORITY ENCODERS

typical performance

TYPE	POWER	DELAY
'148	190 mW	12 ns
'LS148	60 mW	15 ns

SN54148 (J,FH) SN74148 (J,N)
SN54LS148 (J,FH) SN74LS148 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	4	9	A0	1	nc	11	nc
2	5	10	0	2	4	12	A0
3	6	11	1	3	5	13	0
4	7	12	2	4	6	14	1
5	E1	13	3	5	7	15	2
6	A2	14	GS	6	nc	16	nc
7	A1	15	EO	7	E1	17	3
8	GND	16	V_{CC}	8	A2	18	GS
				9	A1	19	EO
				10	GND	20	V_{CC}

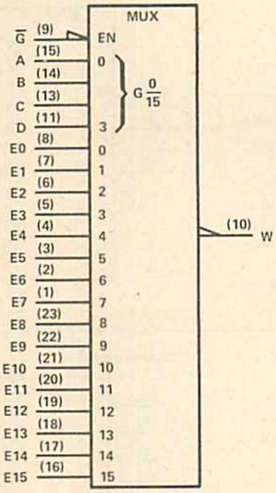
150

1-OF-16 DATA SELECTORS/ MULTIPLEXERS

TYPE	DATA TO INV OUTPUT	FROM ENABLE	TOTAL POWER
'150	11 ns	18 ns	200 mW

SN54150 (J,FH) SN74150 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	E7	13	C	1	nc	15	nc
2	E6	14	B	2	E7	16	C
3	E5	15	A	3	E6	17	B
4	E4	16	E15	4	E5	18	A
5	E3	17	E14	5	E4	19	E15
6	E2	18	E13	6	E3	20	E14
7	E1	19	E12	7	E2	21	E13
8	E0	20	E11	8	nc	22	nc
9	$\overline{G}$	21	E10	9	E1	23	E12
10	W	22	E9	10	E0	24	E11
11	D	23	E8	11	$\overline{G}$	25	E10
12	GND	24	V_{CC}	12	W	26	E9
				13	D	27	E8
				14	GND	28	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

151

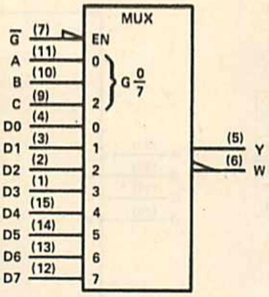
1-OF-8 DATA SELECTORS/MULTIPLEXERS

typical performance

TYPE	DELAY TIMES			TOTAL POWER
	DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE	
'151A	8 ns	16 ns	22 ns	145 mW
'ALS151	6 ns	5 ns	4.5 ns	30 mW
'AS151	3 ns	3.5 ns	5 ns	130 mW
'LS151	11 ns	18 ns	27 ns	30 mW
'S151	4.5 ns	8 ns	9 ns	225 mW

SN54151A (J,FH)	SN74151A (J,N)
SN54ALS151 (J,FH)	SN74ALS151 (N,FN)
SN54AS151 (J,FH)	SN74AS151 (N,FN)
SN54LS151 (J,FH)	SN74LS151 (J,N,FN)
SN54S151 (J,FH)	SN74S151 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D3	9	C	1	nc	11	nc
2	D2	10	B	2	D3	12	C
3	D1	11	A	3	D2	13	B
4	D0	12	D7	4	D1	14	A
5	Y	13	D6	5	D0	15	D7
6	W	14	D5	6	nc	16	nc
7	$\overline{G}$	15	D4	7	Y	17	D6
8	GND	16	V_{CC}	8	W	18	D5
				9	$\overline{G}$	19	D4
				10	GND	20	V_{CC}

152

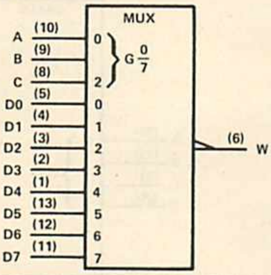
1-of-8 DATA SELECTORS/MULTIPLEXERS

typical performance

TYPE	DELAY TIMES		TOTAL POWER
	DATA TO INV OUTPUT	FROM ENABLE	
'152A	8 ns		130 mW
'LS152	11 ns	18 ns	28 mW

SN54152A (J,FH)
SN54LS152 (J,FH)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D4	8	C	1	nc	11	nc
2	D3	9	B	2	D4	12	C
3	D2	10	A	3	D3	13	B
4	D1	11	D7	4	D2	14	A
5	D0	12	D6	5	nc	15	nc
6	W	13	D5	6	D1	16	D7
7	GND	14	V_{CC}	7	nc	17	nc
				8	D0	18	D6
				9	W	19	D5
				10	GND	20	V_{CC}

153

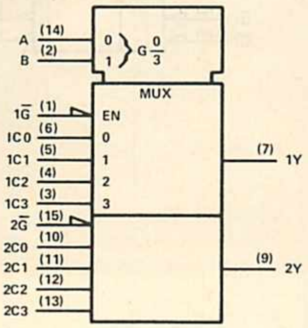
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

typical performance

TYPE	DELAY TIMES		TOTAL POWER
	DATA TO NON-INV OUTPUT	FROM ENABLE	
'153	14 ns	17 ns	180 mW
'ALS153	5 ns	4.5 ns	31.5 mW
'AS153	3.5 ns	5 ns	105 mW
'L153	27 ns	34 ns	90 mW
'LS153	14 ns	17 ns	31 mW
'S153	6 ns	9.5 ns	225 mW

SN54153 (J,FH)	SN74153 (J,N)
SN54ALS153 (J,FH)	SN74ALS153 (N,FN)
SN54AS153 (J,FH)	SN74AS153 (N,FN)
SN54L153 (J)	
SN54LS153 (J,FH)	SN74LS153 (J,N,FN)
SN54S153 (J,FH)	SN74S153 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1$\overline{G}$	9	2Y	1	nc	11	nc
2	B	10	2C0	2	1$\overline{G}$	12	2Y
3	1C3	11	2C1	3	B	13	2C0
4	1C2	12	2C2	4	1C3	14	2C1
5	1C1	13	2C3	5	1C2	15	2C2
6	1C0	14	A	6	nc	16	nc
7	1Y	15	2$\overline{G}$	7	1C1	17	2C3
8	GND	16	V_{CC}	8	1C0	18	A
				9	1Y	19	2$\overline{G}$
				10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

154

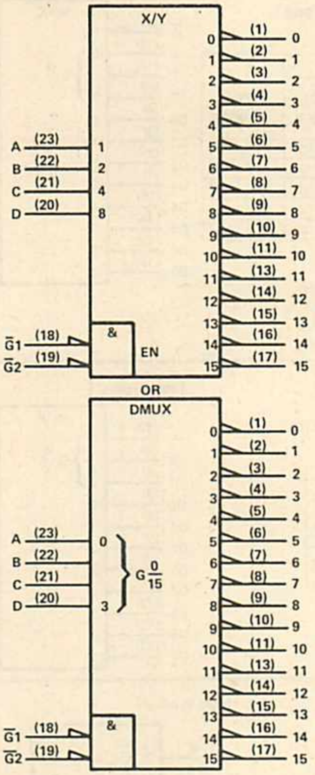
4-LINE TO 16-LINE DECODERS/ DEMULTIPLEXERS

typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'154	23 ns	19 ns	170 mW
'L154	46 ns	38 ns	85 mW

SN54154 (J,FH) SN74154 (J,N)
SN54L154 (J)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	0	13	11	1	nc	15	nc
2	1	14	12	2	0	16	11
3	2	15	13	3	1	17	12
4	3	16	14	4	2	18	13
5	4	17	15	5	3	19	14
6	5	18	$\overline{G}1$	6	4	20	15
7	6	19	$\overline{G}2$	7	5	21	$\overline{G}1$
8	7	20	D	8	nc	22	nc
9	8	21	C	9	6	23	$\overline{G}2$
10	9	22	B	10	7	24	D
11	10	23	A	11	8	25	C
12	GND	24	V_{CC}	12	9	26	B
				13	10	27	A
				14	GND	28	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

155

DECODERS/DEMULTIPLEXERS

(totem pole outputs)

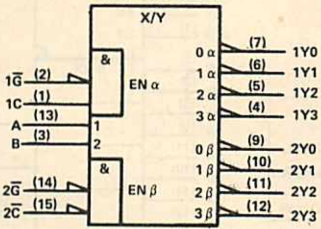
typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'155	21 ns	16 ns	125 mW
'LS155A	18 ns	15 ns	30 mW

SN54155 (J,FH) SN74155 (J,N)
SN54LS155A (J, FH) SN74LS155A, (J, N, FN)

logic symbol†

2-line to 4-line Decoder



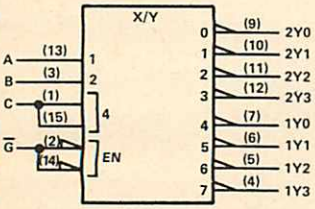
pin assignments

J, N PACKAGES			
1	1C	9	2Y0
2	$1\overline{G}$	10	2Y1
3	B	11	2Y2
4	1Y3	12	2Y3
5	1Y2	13	A
6	1Y1	14	$2\overline{G}$
7	1Y0	15	$2\overline{C}$
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1C	12	2Y0
3	$1\overline{G}$	13	2Y1
4	B	14	2Y2
5	1Y3	15	2Y3
6	nc	16	nc
7	1Y2	17	A
8	1Y1	18	$2\overline{G}$
9	1Y0	19	$2\overline{C}$
10 ·	GND	20	V_{CC}

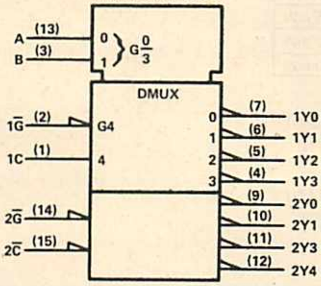
logic symbol†

3-line to 8-line Decoder



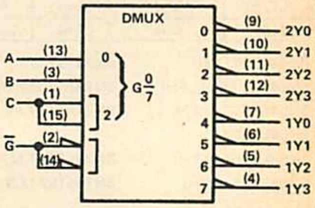
logic symbol†

1-line to 4-line DMUX



logic symbol†

1-line to 8-line DMUX



156

DECODERS/DEMULTIPLEXERS

(open-collector outputs)

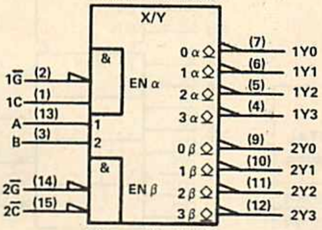
typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'156	23 ns	18 ns	125 mW
'LS156	33 ns	26 ns	31 mW

SN54156 (J,FH) SN74156 (J,N)
SN54LS156 (J,FH) SN74LS156 (J,N,FN)

logic symbol†

2-line to 4-line Decoder

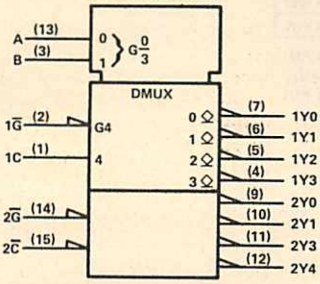


pin assignments

J, N PACKAGES			
1	1C	9	2Y0
2	$1\overline{G}$	10	2Y1
3	B	11	2Y2
4	1Y3	12	2Y3
5	1Y2	13	A
6	1Y1	14	$2\overline{G}$
7	1Y0	15	$2\overline{C}$
8	GND	16	V_{CC}

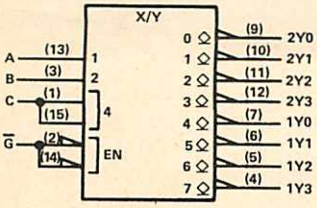
FH, FN PACKAGES			
1	nc	11	nc
2	1C	12	2Y0
3	$1\overline{G}$	13	2Y1
4	B	14	2Y2
5	1Y3	15	2Y3
6	nc	16	nc
7	1Y2	17	A
8	1Y1	18	$2\overline{G}$
9	1Y0	19	$2\overline{C}$
10	GND	20	V_{CC}

1-line to 4-line DMUX



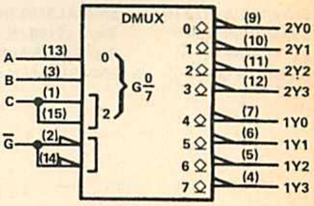
logic symbol†

3-line to 8-line Decoder



logic symbol†

1-line to 8-line DMUX



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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

157

QUAD 2- TO 1-LINE DATA SELECTORS/MULTIPLEXERS

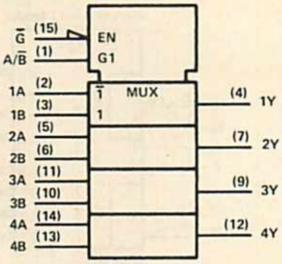
(non-inverted data outputs)

typical performance

TYPE	DELAY TIMES		TOTAL POWER
	DATA TO NON-INV OUTPUT	FROM ENABLE	
'157	9 ns	14 ns	150 mW
'ALS157	5 ns	6.5 ns	39 mW
'AS157	3.5 ns	7.5 ns	95 mW
'L157	18 ns	27 ns	75 mW
'LS157	9 ns	14 ns	49 mW
'S157	5 ns	8 ns	250 mW

SN54157 (J,FH)	SN74157 (J,N)
SN54ALS157 (J,FH)	SN74ALS157 (N,FN)
SN54AS157 (J,FH)	SN74AS157 (N,FN)
SN54L157 (J)	
SN54LS157 (J,FH)	SN74LS157 (J,N,FN)
SN54S157 (J,FH)	SN74S157 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A/$\overline{B}$	9	3Y	1	nc	11	nc
2	1A	10	3B	2	A/$\overline{B}$	12	3Y
3	1B	11	3A	3	1A	13	3B
4	1Y	12	4Y	4	1B	14	3A
5	2A	13	4B	5	1Y	15	4Y
6	2B	14	4A	6	nc	16	nc
7	2Y	15	$\overline{G}$	7	2A	17	4B
8	GND	16	V_{CC}	8	2B	18	4A
				9	2Y	19	$\overline{G}$
				10	GND	20	V_{CC}

158

QUAD 2- TO 1-LINE DATA SELECTORS/MULTIPLEXERS

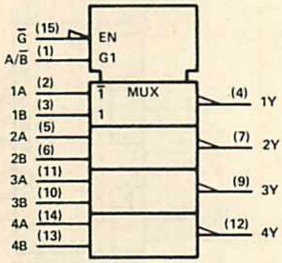
(inverted data outputs)

typical performance

TYPE	DELAY TIMES		TOTAL POWER
	DATA TO INV OUTPUT	FROM ENABLE	
'ALS158	5 ns	6.5 ns	11.5 mW
'AS158	1.2 ns	6 ns	78 mW
'LS158	7 ns	12 ns	24 mW
'S158	4 ns	7 ns	195 mW

SN54ALS158 (J,FH)	SN74ALS158 (N,FN)
SN54AS158 (J,FH)	SN74AS158 (N,FN)
SN54LS158 (J,FH)	SN74LS158 (J,N,FN)
SN54S158 (J,FH)	SN74S158 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A/$\overline{B}$	9	3Y	1	nc	11	nc
2	1A	10	3B	2	A/$\overline{B}$	12	3Y
3	1B	11	3A	3	1A	13	3B
4	1Y	12	4Y	4	1B	14	3A
5	2A	13	4B	5	1Y	15	4Y
6	2B	14	4A	6	nc	16	nc
7	2Y	15	$\overline{G}$	7	2A	17	4B
8	GND	16	V_{CC}	8	2B	18	4A
				9	2Y	19	$\overline{G}$
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

159

4- TO 16-LINE DECODERS/ DEMULTIPLEXERS

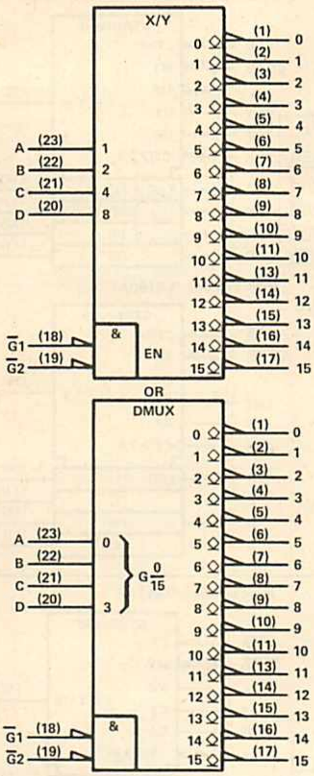
(open-collector outputs)

typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'159	24 ns	19 ns	170 mW

SN54159 (J,FH) SN74159 (J,N)

logic symbol, '159†



pin assignments

J, N PACKAGES			
1	0	13	11
2	1	14	12
3	2	15	13
4	3	16	14
5	4	17	15
6	5	18	$\overline{G}1$
7	6	19	$\overline{G}2$
8	7	20	D
9	8	21	C
10	9	22	B
11	10	23	A
12	GND	24	V_{CC}

FH PACKAGE'			
1	nc	15	nc
2	0	16	11
3	1	17	12
4	2	18	13
5	3	19	14
6	4	20	15
7	5	21	$\overline{G}1$
8	nc	22	nc
9	6	23	$\overline{G}2$
10	7	24	D
11	8	25	C
12	9	26	B
13	10	27	A
14	GND	28	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

160

SYNCHRONOUS 4-BIT COUNTERS

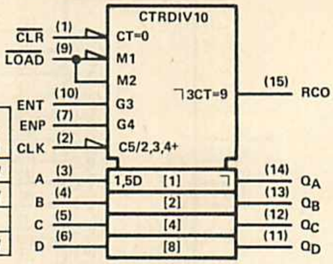
(decade, direct clear)

typical performance

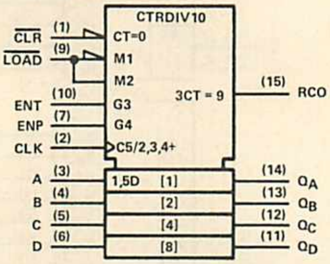
TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'160	25 MHz	ASYNC-L	305 mW
'ALS160A	40 MHz	ASYNC-L	60 mW
'AS160		ASYNC-L	
'LS160A	25 MHz	ASYNC-L	93 mW

SN54160 (J,FH)	SN74160 (J,N)
SN54ALS160A (J,FH)	SN74ALS160A (N,FN)
SN54AS160 (J,FH)	SN74AS160 (N,FN)
SN54LS160A (J,FH)	SN74LS160A (J,N,FN)

logic symbol, '160†



logic symbol, 'LS160A†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CLR}$	9	$\overline{LOAD}$	1	nc	11	nc
2	CLK	10	ENT	2	$\overline{CLR}$	12	$\overline{LOAD}$
3	A	11	Q_D	3	CLK	13	ENT
4	B	12	Q_C	4	A	14	Q_D
5	C	13	Q_B	5	B	15	Q_C
6	D	14	Q_A	6	nc	16	nc
7	ENP	15	RCO	7	C	17	Q_B
8	GND	16	V_{CC}	8	D	18	Q_A
				9	ENP	19	RCO
				10	GND	20	V_{CC}

161

SYNCHRONOUS 4-BIT COUNTERS

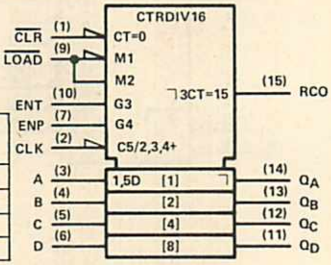
(binary, direct clear)

typical performance

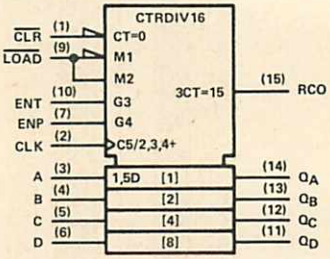
TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'161	25 MHz	ASYNC-L	305 mW
'ALS161A	40 MHz	ASYNC-L	60 mW
'AS161		ASYNC-L	
'LS161A	25 MHz	ASYNC-L	93 mW

SN54161 (J,FH)	SN74161 (J,N)
SN54ALS161A (J,FH)	SN74ALS161A (N,FN)
SN54AS161 (J,FH)	SN74AS161 (N,FN)
SN54LS161A (J,FH)	SN74LS161A (J,N,FN)

logic symbol, '161†



logic symbol, 'LS161A†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CLR}$	9	$\overline{LOAD}$	1	nc	11	nc
2	CLK	10	ENT	2	$\overline{CLR}$	12	$\overline{LOAD}$
3	A	11	Q_D	3	CLK	13	ENT
4	B	12	Q_C	4	A	14	Q_D
5	C	13	Q_B	5	B	15	Q_C
6	D	14	Q_A	6	nc	16	nc
7	ENP	15	RCO	7	C	17	Q_B
8	GND	16	V_{CC}	8	D	18	Q_A
				9	ENP	19	RCO
				10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

162

SYNCHRONOUS 4-BIT COUNTERS

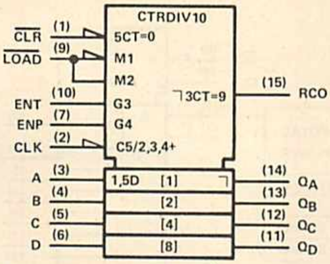
(decade, synchronous clear)

typical performance

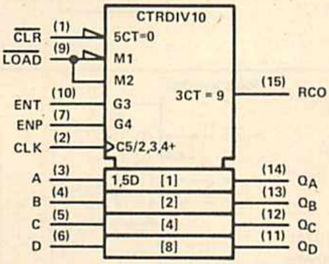
TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'162	25 MHz	SYNC-L	305 mW
'ALS162A	40 MHz	SYNC-L	60 mW
'AS162		SYNC-L	
'LS162A	25 MHz	SYNC-L	93 mW
'S162	40 MHz	SYNC-L	475 mW

SN54162 (J,FH)	SN74162 (J,N)
SN54ALS162A (J,FH)	SN74ALS162A (N,FN)
SN54AS162 (J,FH)	SN74AS162 (N,FN)
SN54LS162A (J,FH)	SN74LS162A (J,N,FN)
SN54S162 (J,FH)	SN74S162 (J,N,FN)

logic symbol, '162†



logic symbol, 'LS162A, 'S162†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CLR}$	9	$\overline{LOAD}$	1	nc	11	nc
2	CLK	10	ENT	2	$\overline{CLR}$	12	$\overline{LOAD}$
3	A	11	Q_D	3	CLK	13	ENT
4	B	12	Q_C	4	A	14	Q_D
5	C	13	Q_B	5	B	15	Q_C
6	D	14	Q_A	6	nc	16	nc
7	ENP	15	RCO	7	C	17	Q_B
8	GND	16	V_{CC}	8	D	18	Q_A
				9	ENP	19	RCO
				10	GND	20	V_{CC}

163

SYNCHRONOUS 4-BIT COUNTERS

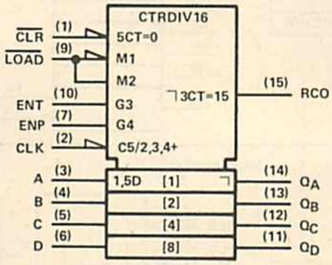
(binary, synchronous clear)

typical performance

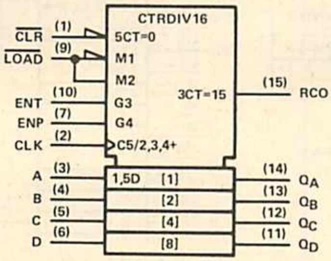
TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'163	25 MHz	SYNC-L	305 mW
'ALS163A	40 MHz	SYNC-L	60 mW
'AS163		SYNC-L	
'LS163A	25 MHz	SYNC-L	93 mW
'S163	40 MHz	SYNC-L	475 mW

SN54163 (J,FH)	SN74163 (J,N)
SN54ALS163A (J,FH)	SN74ALS163A (N,FN)
SN54AS163 (J,FH)	SN74AS163 (N,FN)
SN54LS163A (J,FH)	SN74LS163A (J,N,FN)
SN54S163 (J,FH)	SN74S163 (J,N,FN)

logic symbol, '163†



logic symbol, 'LS163A, 'S163†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CLR}$	9	$\overline{LOAD}$	1	nc	11	nc
2	CLK	10	ENT	2	$\overline{CLR}$	12	$\overline{LOAD}$
3	A	11	Q_D	3	CLK	13	ENT
4	B	12	Q_C	4	A	14	Q_D
5	C	13	Q_B	5	B	15	Q_C
6	D	14	Q_A	6	nc	16	nc
7	ENP	15	RCO	7	C	17	Q_B
8	GND	16	V_{CC}	8	D	18	Q_A
				9	ENP	19	RCO
				10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

164

8-BIT PARALLEL OUT SERIAL SHIFT REGISTERS

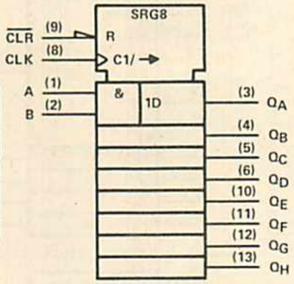
(asynchronous clear)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'164	25 MHz	GATED D	LOW	167 mW
'ALS164		GATED D	LOW	
'L164	12 MHz	GATED D	LOW	84 mW
'LS164	25 MHz	GATED D	LOW	80 mW

SN54164 (J,FH) SN74164 (J,N)
SN54ALS164 (J,FH) SN74ALS164 (N,FN)
SN54L164 (J)
SN54LS164 (J,FH) SN74LS164 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A	8	CLK	1	nc	11	nc
2	B	9	$\overline{CLR}$	2	A	12	CLK
3	Q_A	10	Q_E	3	B	13	$\overline{CLR}$
4	Q_B	11	Q_F	4	Q_A	14	Q_E
5	Q_C	12	Q_G	5	nc	15	nc
6	Q_D	13	Q_H	6	Q_B	16	Q_F
7	GND	14	V_{CC}	7	nc	17	nc
				8	Q_C	18	Q_G
				9	Q_D	19	Q_H
				10	GND	20	V_{CC}

165

8-BIT SHIFT REGISTERS

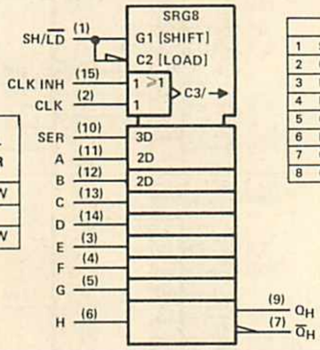
(parallel-load with complementary outputs)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'165	25 MHz	D	NONE	210 mW
'ALS165				
'LS165	35 MHz	D	NONE	105 mW

SN54165 (J,FH) SN74165 (J,N)
SN54ALS165 (J,FH) SN74ALS165 (N,FN)
SN54LS165 (J,FH) SN74LS165 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	SH/$\overline{LD}$	9	Q_H	1	nc	11	nc
2	CLK	10	SER	2	SH/$\overline{LD}$	12	Q_H
3	E	11	A	3	CLK	13	SER
4	F	12	B	4	E	14	A
5	G	13	C	5	F	15	B
6	H	14	D	6	nc	16	nc
7	$\overline{Q}_H$	15	CLK INH	7	G	17	C
8	GND	16	V_{CC}	8	H	18	D
				9	$\overline{Q}_H$	19	CLK INH
				10	GND	20	V_{CC}

166

8-BIT SHIFT REGISTERS

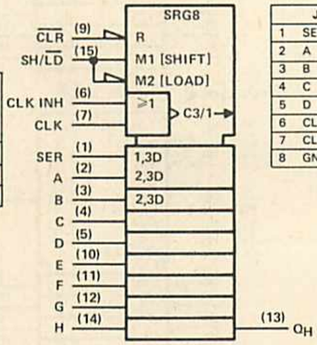
(parallel/serial input; serial output)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'166	20 MHz	D	LOW	360 mW
'ALS166		D	LOW	
'LS166A	35 MHz	D	LOW	110 mW

SN54166 (J,FH) SN74166 (J,N)
SN54ALS166 (J,FH) SN74ALS166 (N,FN)
SN54LS166A (J,FH) SN74LS166A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	SER	9	$\overline{CLR}$	1	nc	11	nc
2	A	10	E	2	SER	12	$\overline{CLR}$
3	B	11	F	3	A	13	E
4	C	12	G	4	B	14	F
5	D	13	Q_H	5	C	15	G
6	CLK INH	14	H	6	nc	16	nc
7	CLK	15	SH/$\overline{LD}$	7	D	17	Q_H
8	GND	16	V_{CC}	8	CLK INH	18	H
				9	CLK	19	SH/$\overline{LD}$
				10	GND	20	V_{CC}

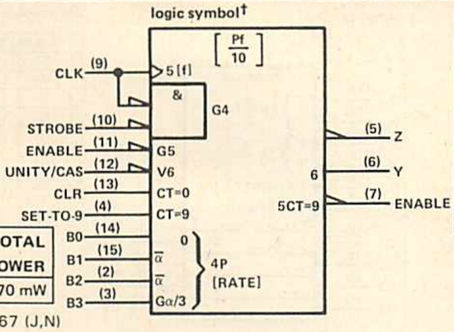
† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

167

SYNCHRONOUS DECADE RATE MULTIPLIERS

logic symbol†



pin assignments

J, N PACKAGES				FH PACK			
1	nc	9	CLK	1	nc	1	
2	B2	10	STRB	2	nc	12	
3	B3	11	ENin	3	B2	13	
4	SET-TO-9	12	UNITY/CAS	4	B3	14	
5	Z	13	CLR	5	SET-TO-9	15	
6	Y	14	B0	6	nc	16	nc
7	ENout	15	B1	7	Z	17	CL
8	GND	16	V_{CC}	8	Y	18	B0
				9	ENout	19	B1
				10	GND	20	V_{CC}

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'167	25 MHz	ASYNC-H	270 mW

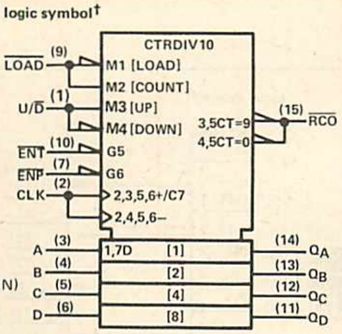
SN54167 (J,FH) SN74167 (J,N)

168

4-BIT UP/DOWN SYNCHRONOUS COUNTERS

(decade)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$U/\overline{D}$	9	$\overline{\text{LOAD}}$	1	nc	11	nc
2	CLK	10	$\overline{\text{ENT}}$	2	$U/\overline{D}$	12	$\overline{\text{LOAD}}$
3	A	11	Q_D	3	CLK	13	$\overline{\text{ENT}}$
4	B	12	Q_C	4	A	14	Q_D
5	C	13	Q_B	5	B	15	Q_C
6	D	14	Q_A	6	nc	16	nc
7	$\overline{\text{ENP}}$	15	$\overline{\text{RCO}}$	7	C	17	Q_B
8	GND	16	V_{CC}	8	D	18	Q_A
				9	$\overline{\text{ENP}}$	19	$\overline{\text{RCO}}$
				10	GND	20	V_{CC}

typical performance

TYPE	COUNT FREQ	TOTAL POWER
'ALS168A	40 MHz	75 mW
'AS168		
'S168	40 MHz	500 mW

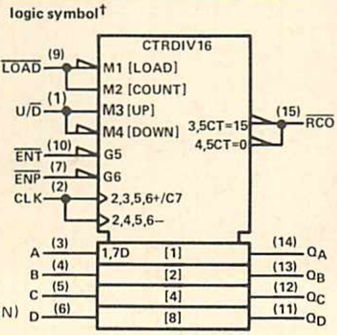
SN54ALS168A (J,FH) SN74ALS168A (N,FN)
SN54AS168 (J,FH) SN74AS168 (N,FN)
SN54S168 (J,FH) SN74S168 (J,N,FN)

169

4-BIT UP/DOWN SYNCHRONOUS COUNTERS

(binary)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$U/\overline{D}$	9	$\overline{\text{LOAD}}$	1	nc	11	nc
2	CLK	10	$\overline{\text{ENT}}$	2	$U/\overline{D}$	12	$\overline{\text{LOAD}}$
3	A	11	Q_D	3	CLK	13	$\overline{\text{ENT}}$
4	B	12	Q_C	4	A	14	Q_D
5	C	13	Q_B	5	B	15	Q_C
6	D	14	Q_A	6	nc	16	nc
7	$\overline{\text{ENP}}$	15	$\overline{\text{RCO}}$	7	C	17	Q_B
8	GND	16	V_{CC}	8	D	18	Q_A
				9	$\overline{\text{ENP}}$	19	$\overline{\text{RCO}}$
				10	GND	20	V_{CC}

typical performance

TYPE	COUNT FREQ	TOTAL POWER
'ALS169A	40 MHz	75 mW
'AS169		
'LS169B	35 MHz	140 mW
'S169	40 MHz	500 mW

SN54ALS169A (J,FH) SN74ALS169A (N,FN)
SN54AS169 (J,FH) SN74AS169 (N,FN)
SN54LS169B (J,FH) SN74LS169B (J,N,FN)
SN54S169 (J,FH) SN74S169 (J,N,FN)

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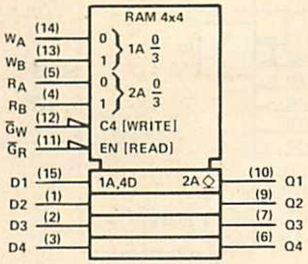
† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

OWER PER BIT
40 mW
7.8 mW

SN74170 (J,N)
SN74LS170 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D2	9	Q2	1	nc	11	nc
2	D3	10	Q1	2	D2	12	Q2
3	D4	11	$\overline{G}_R$	3	D3	13	Q1
4	R_B	12	$\overline{G}_W$	4	D4	14	$\overline{G}_R$
5	R_A	13	W_B	5	R_B	15	$\overline{G}_W$
6	Q4	14	W_A	6	nc	16	nc
7	Q3	15	D1	7	R_A	17	W_B
8	GND	16	V_{CC}	8	Q4	18	W_A
				9	Q3	19	D1
				10	GND	20	V_{CC}

D D-TYPE FLIP-FLOPS WITH CLEAR

- Double-Rail Outputs
- Buffered Clock and Clear Inputs
- Individual Data Inputs to Each Flip-Flop

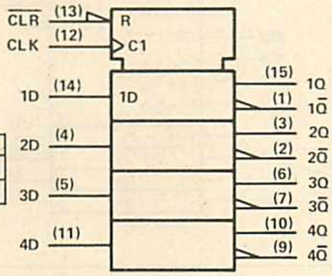
typical performance

TYPE	FREQ	POWER PER F-F	DELAY TIMES	
			SETUP	HOLD
'LS171	30 MHz	17.5 mW	20 ns↑	5 ns↑

↑ Rising edge of clock pulse

SN54LS171 (J,FH) SN74LS171 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$1\overline{Q}$	9	$4\overline{Q}$	1	nc	11	nc
2	$2\overline{Q}$	10	4Q	2	$1\overline{Q}$	12	$4\overline{Q}$
3	2Q	11	4D	3	$2\overline{Q}$	13	4Q
4	2D	12	CLK	4	2Q	14	4D
5	3D	13	$\overline{CLR}$	5	2D	15	CLK
6	3Q	14	1D	6	nc	16	nc
7	$3\overline{Q}$	15	1Q	7	3D	17	$\overline{CLR}$
8	GND	16	V_{CC}	8	3Q	18	1D
				9	$3\overline{Q}$	19	1Q
				10	GND	20	V_{CC}

For chip carrier information, contact the factory.

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

172

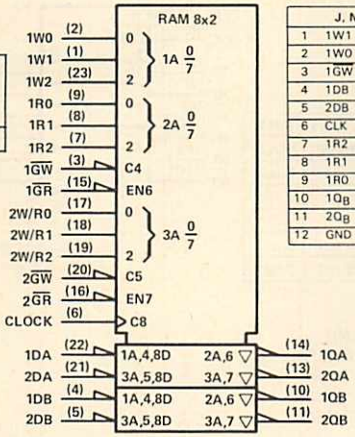
16-BIT REGISTER FILES

typical performance

TYPE	ORG	TYPE OF OUTPUT	ADDRESS TIME	POWER PER BIT
'172	8X2	3-State	33 ns	35 mW

SN74172 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1W1	13	$2Q_A$
2	1W0	14	$1Q_A$
3	1$\overline{GW}$	15	1$\overline{GR}$
4	1DB	16	2$\overline{GR}$
5	2DB	17	2W/R0
6	CLK	18	2W/R1
7	1R2	19	2W/R2
8	1R1	20	2$\overline{GW}$
9	1R0	21	2DA
10	$1Q_B$	22	1DA
11	$2Q_B$	23	1W2
12	GND	24	V_{CC}

173

4-BIT D-TYPE REGISTERS

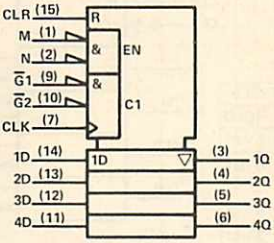
(3-state outputs)

typical performance

TYPE	FREQ	ASYNC CLEAR	TOTAL POWER
'173	25 MHz	HIGH	250 mW
'LS173A	50 MHz	HIGH	85 mW

SN54173 (J,FH) SN74173 (J,N)
SN54LS173A (J,FH) SN74LS173A (J,N,FN)

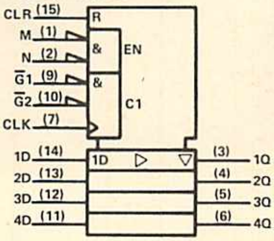
logic symbol, '173†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	M	9	$\overline{G}$1	1	nc	11	nc
2	N	10	$\overline{G}$2	2	M	12	$\overline{G}$1
3	1Q	11	4D	3	N	13	$\overline{G}$2
4	2Q	12	3D	4	1Q	14	4D
5	3Q	13	2D	5	2Q	15	3D
6	4Q	14	1D	6	nc	16	nc
7	CLK	15	CLR	7	3Q	17	2D
8	GND	16	V_{CC}	8	4Q	18	1D
				9	CLK	19	CLR
				10	GND	20	V_{CC}

logic symbol, 'LS173A†



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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

174

HEX D-TYPE FLIP-FLOPS

(single-rail outputs, common direct clear)

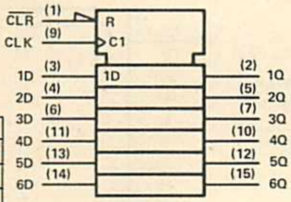
typical performance

TYPE	FREQ	POWER PER F-F	DELAY TIMES	
			SETUP	HOLD
'174	35 MHz	38 mW	20 ns†	5 ns†
'ALS174	80 MHz	6.7 mW	15 ns†	0 ns†
'AS174	175 MHz	38 mW		
'LS174	40 MHz	10.6 mW	20 ns†	5 ns†
'S174	110 MHz	75 mW	5 ns†	3 ns†

† Rising edge of clock pulse

SN54174 (J,FH)	SN74174 (J,N)
SN54ALS174 (J,FH)	SN74ALS174 (N,FN)
SN54AS174 (J,FH)	SN74AS174 (N,FN)
SN54LS174 (J,FH)	SN74LS174 (J,N,FN)
SN54S174 (J,FH)	SN74S174 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{\text{CLR}}$	9	CLK	1	nc	11	nc
2	1Q	10	4Q	2	$\overline{\text{CLR}}$	12	CLK
3	1D	11	4D	3	1Q	13	4Q
4	2D	12	5Q	4	1D	14	4D
5	2Q	13	5D	5	2D	15	5Q
6	3D	14	6D	6	nc	16	nc
7	3Q	15	6Q	7	2Q	17	5D
8	GND	16	V_{CC}	8	3D	18	6D
				9	3Q	19	6Q
				10	GND	20	V_{CC}

175

QUAD D-TYPE FLIP-FLOPS

(complementary outputs, common direct clear)

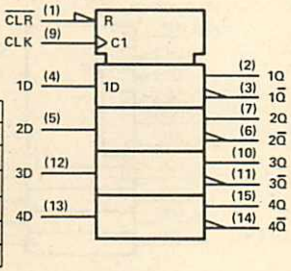
typical performance

TYPE	FREQ	POWER PER F-F	DELAY TIMES	
			SETUP	HOLD
'175	35 MHz	38 mW	20 ns†	5 ns†
'ALS175	80 MHz	7.5 mW	15 ns†	0 ns†
'AS175	175 MHz	41 mW		
'LS175	40 MHz	10.6 mW	20 ns†	5 ns†
'S175	110 MHz	75 mW	5 ns†	3 ns†

† Rising edge of clock pulse

SN54175 (J,FH)	SN74175 (J,N)
SN54ALS175 (J,FH,	SN74ALS175 (N,FN)
SN54AS175 (J,FH)	SN74AS175 (N,FN)
SN54LS175 (J,FH)	SN74LS175 (J,N,FN)
SN54S175 (J,FH)	SN74S175 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{\text{CLR}}$	9	CLK	1	nc	11	nc
2	1Q	10	3Q	2	$\overline{\text{CLR}}$	12	CLK
3	$1\overline{Q}$	11	$3\overline{Q}$	3	1Q	13	3Q
4	1D	12	3D	4	$1\overline{Q}$	14	$3\overline{Q}$
5	2D	13	4D	5	1D	15	3D
6	$2\overline{Q}$	14	$4\overline{Q}$	6	nc	16	nc
7	2Q	15	4Q	7	2D	17	4D
8	GND	16	V_{CC}	8	$2\overline{Q}$	18	$4\overline{Q}$
				9	2Q	19	4Q
				10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

176

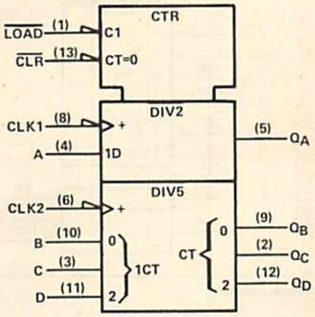
PRESETTABLE DECADE/ BIQUINARY COUNTERS

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'176	35 MHz	LOW	150 mW

SN54176 (J,FH) SN74176 (J,N)

logic symbol, '176†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	$\overline{\text{LOAD}}$	8	CLK1	1	nc	11	nc
2	Q_C	9	Q_B	2	$\overline{\text{LOAD}}$	12	CLK1
3	C	10	B	3	Q_C	13	Q_B
4	A	11	D	4	C	14	B
5	Q_A	12	Q_D	5	nc	15	nc
6	CLK2	13	$\overline{\text{CLR}}$	6	A	16	D
7	GND	14	V_{CC}	7	nc	17	nc
				8	Q_A	18	Q_D
				9	CLK2	19	$\overline{\text{CLR}}$
				10	GND	20	V_{CC}

177

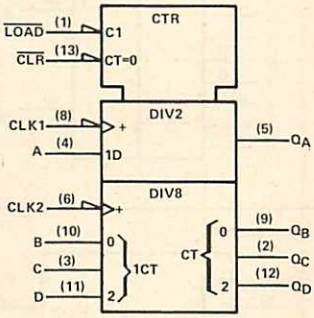
PRESETTABLE BINARY COUNTERS

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'177	35 MHz	LOW	150 mW

SN54177 (J,FH) SN74177 (J,N)

logic symbol, '177†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	$\overline{\text{LOAD}}$	8	CLK1	1	nc	11	nc
2	Q_C	9	Q_B	2	$\overline{\text{LOAD}}$	12	CLK1
3	C	10	B	3	Q_C	13	Q_B
4	A	11	D	4	C	14	B
5	Q_A	12	Q_D	5	nc	15	nc
6	CLK2	13	$\overline{\text{CLR}}$	6	A	16	D
7	GND	14	V_{CC}	7	nc	17	nc
				8	Q_A	18	Q_D
				9	CLK2	19	$\overline{\text{CLR}}$
				10	GND	20	V_{CC}

178

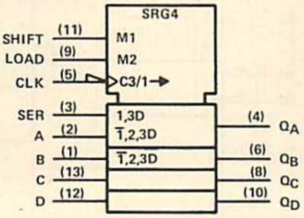
4-BIT UNIVERSAL SHIFT REGISTER

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'178	25 MHz	D	NONE	230 mW

SN54178 (J,FH) SN74178 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	B	8	Q_C	1	nc	11	nc
2	A	9	LOAD	2	B	12	Q_C
3	SER	10	Q_D	3	A	13	LOAD
4	Q_A	11	SHIFT	4	SER	14	Q_D
5	CLK	12	D	5	nc	15	nc
6	Q_B	13	C	6	Q_A	16	SHIFT
7	GND	14	V_{CC}	7	nc	17	nc
				8	CLK	18	D
				9	Q_B	19	C
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

179

4-BIT UNIVERSAL SHIFT REGISTERS

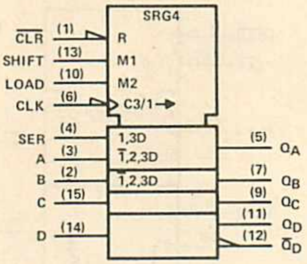
(direct clear; Q_D complementary outputs)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'179	25 MHz	D	LOW	230 mW

SN54179 (J,FH) SN74179 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	$\overline{CLR}$	9	Q_C	1	nc	11	nc
2	B	10	LOAD	2	$\overline{CLR}$	12	Q_C
3	A	11	Q_D	3	B	13	LOAD
4	SER	12	$\overline{Q}_D$	4	A	14	Q_D
5	Q_A	13	SHIFT	5	SER	15	$\overline{Q}_D$
6	CLK	14	D	6	nc	16	nc
7	Q_B	15	C	7	Q_A	17	SHIFT
8	GND	16	V_{CC}	8	CLK	18	D
				9	Q_B	19	C
				10	GND	20	V_{CC}

180

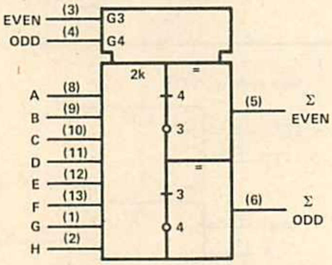
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

typical performance

TYPE	POWER	DELAY
'180	170 mW	35 ns

SN54180 (J,FH) SN74180 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	G	8	A	1	nc	11	nc
2	H	9	B	2	G	12	A
3	EVEN	10	C	3	H	13	B
4	ODD	11	D	4	EVEN	14	C
5	ΣEVEN	12	E	5	nc	15	nc
6	ΣODD	13	F	6	ODD	16	D
7	GND	14	V_{CC}	7	nc	17	nc
				8	ΣEVEN	18	E
				9	ΣODD	19	F
				10	GND	20	V_{CC}

181

ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS

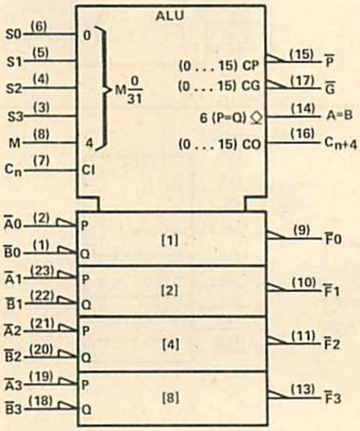
(16 arithmetic operations, 16 logic functions)

typical performance

TYPE	CARRY TIME	ADD TIME	TOTAL POWER
'181	12.5 ns	24 ns	455 mW
'AS181A	6 ns	5 ns	675 mW
'LS181	16 ns	24 ns	102 mW
'S181	7 ns	11 ns	600 mW

SN54181 (J,FH) SN74181 (J,N)
SN54AS181A (J,FH) SN74AS181A (N,FN)
SN54LS181 (J,FH) SN74LS181 (J,N,FN)
SN54S181 (J,FH) SN74S181 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{B}0$	13	$\overline{F}3$	1	nc	15	nc
2	$\overline{A}0$	14	A=B	2	$\overline{B}0$	16	$\overline{F}3$
3	S3	15	$\overline{P}$	3	$\overline{A}0$	17	A=B
4	S2	16	C_{n+4}	4	S3	18	$\overline{P}$
5	S1	17	$\overline{G}$	5	S2	19	C_{n+4}
6	S0	18	$\overline{B}3$	6	S1	20	$\overline{G}$
7	C_n	19	$\overline{A}3$	7	S0	21	$\overline{B}3$
8	M	20	$\overline{B}2$	8	nc	22	nc
9	$\overline{F}0$	21	$\overline{A}2$	9	C_n	23	$\overline{A}3$
10	$\overline{F}1$	22	$\overline{B}1$	10	M	24	$\overline{B}2$
11	$\overline{F}2$	23	$\overline{A}1$	11	$\overline{F}0$	25	$\overline{A}2$
12	GND	24	V_{CC}	12	$\overline{F}1$	26	$\overline{B}1$
				13	$\overline{F}2$	27	$\overline{A}1$
				14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

182

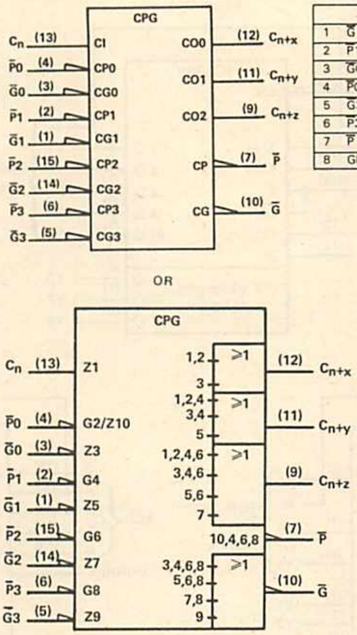
LOOK-AHEAD CARRY GENERATORS

typical performance

TYPE	POWER	CARRY TIME
'182	180 mW	13 ns
'AS182	100 mW	5 ns
'S182	260 mW	7 ns

SN54182 (J,FH) SN74182 (J,N)
SN54AS182 (J,FH) SN74AS182 (N,FN)
SN54S182 (J,FH) SN74S182 (J,N,FN)

logic symbols†



pin assignments

J, N PACKAGES			
1	$\overline{G1}$	9	C_{n+z}
2	$\overline{P1}$	10	$\overline{G}$
3	$\overline{G0}$	11	C_{n+y}
4	$\overline{P0}$	12	C_{n+x}
5	$\overline{G3}$	13	C_n
6	$\overline{P3}$	14	$\overline{G2}$
7	$\overline{P}$	15	$\overline{P2}$
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	$\overline{G1}$	12	C_{n+z}
3	$\overline{P1}$	13	$\overline{G}$
4	$\overline{G0}$	14	C_{n+y}
5	$\overline{P0}$	15	C_{n+x}
6	nc	16	nc
7	$\overline{G3}$	17	C_n
8	$\overline{P3}$	18	$\overline{G2}$
9	$\overline{P}$	19	$\overline{P2}$
10	GND	20	V_{CC}

183

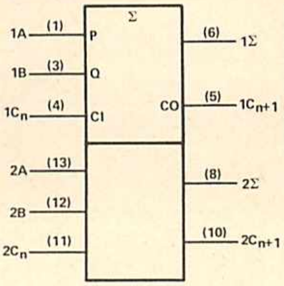
DUAL CARRY-SAVE FULL ADDERS

typical performance

TYPE	CARRY TIME	ADD TIME	POWER PER BIT
'H183	11 ns	11 ns	110 mW
'LS183	15 ns	15 ns	23 mW

SN54H183 (J,FH) SN74H183 (J,N)
SN54LS183 (J,FH) SN74LS183 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1A	8	2Σ
2	nc	9	nc
3	1B	10	$2C_{n+1}$
4	$1C_n$	11	$2C_n$
5	$1C_{n+1}$	12	2B
6	1Σ	13	2A
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	2Σ
3	nc	13	nc
4	1B	14	$2C_{n+1}$
5	nc	15	nc
6	$1C_n$	16	$2C_n$
7	nc	17	nc
8	$1C_{n+1}$	18	2B
9	1Σ	19	2A
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

184

CODE CONVERTERS

(BCD to binary)

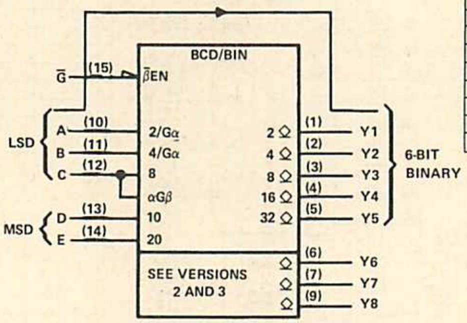
typical performance

TYPE	POWER	DELAY
'184	280 mW	25 ns

SN54184 (J,FH) SN74184 (J,N)

logic symbols†

VERSION 1

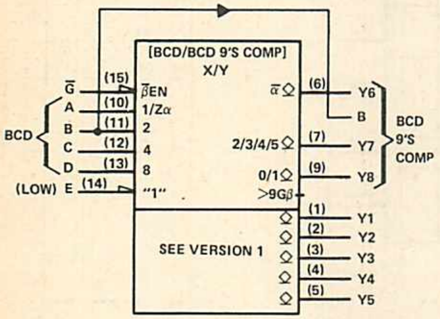


pin assignments

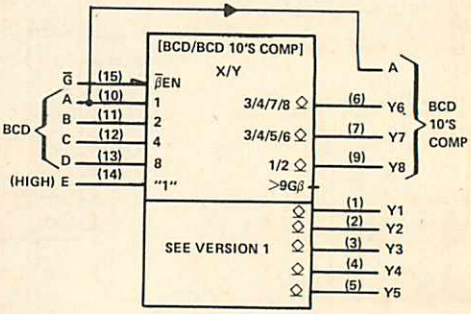
J, N PACKAGES			
1	Y1	9	Y8
2	Y2	10	A
3	Y3	11	B
4	Y4	12	C
5	Y5	13	D
6	Y6	14	E
7	Y7	15	G̅
8	GND	16	V_{CC}

FH PACKAGE			
1	nc	11	nc
2	Y1	12	Y8
3	Y2	13	A
4	Y3	14	B
5	Y4	15	C
6	nc	16	nc
7	Y5	17	D
8	Y6	18	E
9	Y7	19	G̅
10	GND	20	V_{CC}

VERSION 2



VERSION 3



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† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

185

CODE CONVERTERS

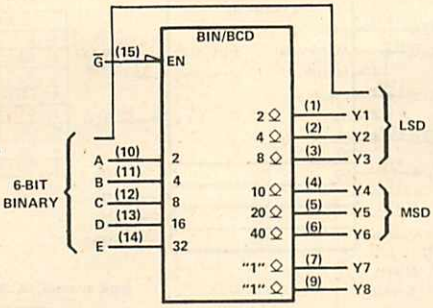
(binary to BCD)

typical performance

TYPE	POWER	DELAY
'185A	280 mW	25 ns

SN54185A (J,FH) SN74185A (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	Y1	9	Y8	1	nc	11	nc
2	Y2	10	A	2	Y1	12	Y8
3	Y3	11	B	3	Y2	13	A
4	Y4	12	C	4	Y3	14	B
5	Y5	13	D	5	Y4	15	C
6	Y6	14	E	6	nc	16	nc
7	Y7	15	$\overline{G}$	7	Y5	17	D
8	GND	16	V_{CC}	8	Y6	18	E
				9	Y7	19	$\overline{G}$
				10	GND	20	V_{CC}

187

1024-BIT READ-ONLY MEMORIES

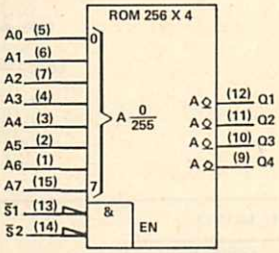
(256 4-bit words; open-collector outputs)

typical performance

TYPE	ACCESS TIMES	
	CHIP-SELECT	ADDRESS
'187	20 ns	40 ns

SN54187 (J,FH) SN74187 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	A6	9	Q4	1	nc	11	nc
2	A5	10	Q3	2	A6	12	Q4
3	A4	11	Q2	3	A5	13	Q3
4	A3	12	Q1	4	A4	14	Q2
5	A0	13	$\overline{S}$1	5	A3	15	Q1
6	A1	14	$\overline{S}$2	6	nc	16	nc
7	A2	15	A7	7	A0	17	$\overline{S}$1
8	GND	16	V_{CC}	8	A1	18	$\overline{S}$2
				9	A2	19	A7
				10	GND	20	V_{CC}

189

64-BIT RANDOM-ACCESS MEMORIES

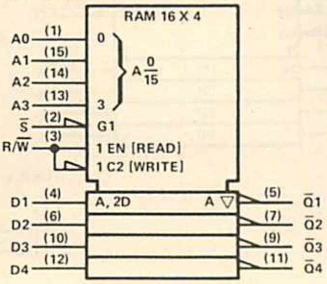
(16 4-bit words; three-state outputs)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER PER BIT
'LS189A	50 ns	35 ns	2.7 mW
'S189B	25 ns	12 ns	5.9 mW

SN54LS189A (J,FH) SN74LS189A (J,N,FN)
SN54S189B (J,FH) SN74S189B (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A0	9	$\overline{Q}$3	1	nc	11	nc
2	$\overline{S}$	10	D3	2	A0	12	$\overline{Q}$3
3	R/$\overline{W}$	11	$\overline{Q}$4	3	$\overline{S}$	13	D3
4	D1	12	D4	4	R/$\overline{W}$	14	$\overline{Q}$4
5	$\overline{Q}$1	13	A3	5	D1	15	D4
6	D2	14	A2	6	nc	16	nc
7	$\overline{Q}$2	15	A1	7	$\overline{Q}$1	17	A3
8	GND	16	V_{CC}	8	D2	18	A2
				9	$\overline{Q}$2	19	A1
				10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

190

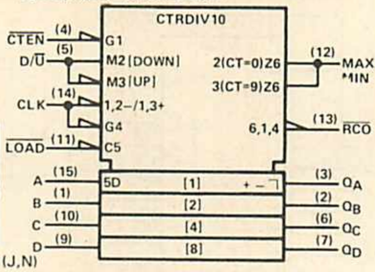
SYNCHRONOUS UP/DOWN COUNTERS (BCD)

typical performance

TYPE	COUNT FREQ	TOTAL POWER
'190	20 MHz	325 mW
'ALS190	35 MHz	60 mW
'LS190	20 MHz	100 mW

SN54190 (J,FH)	SN74190 (J,N)
SN54ALS190 (J,FH)	SN74ALS190 (N,FN)
SN54LS190 (J,FH)	SN74LS190 (J,N,FN)

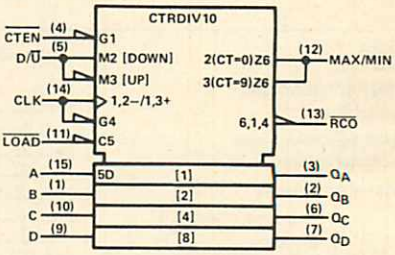
logic symbol,'190, 'LS190†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	D	1	nc	11	nc
2	Q_B	10	C	2	B	12	D
3	Q_A	11	$\overline{\text{LOAD}}$	3	Q_B	13	C
4	$\overline{\text{CTEN}}$	12	MAX/MIN	4	Q_A	14	$\overline{\text{LOAD}}$
5	D/$\overline{\text{U}}$	13	$\overline{\text{RCO}}$	5	$\overline{\text{CTEN}}$	15	MAX/MIN
6	Q_C	14	CLK	6	nc	16	nc
7	Q_D	15	A	7	D/$\overline{\text{U}}$	17	$\overline{\text{RCO}}$
8	GND	16	V_{CC}	8	Q_C	18	CLK
				9	Q_D	19	A
				10	GND	20	V_{CC}

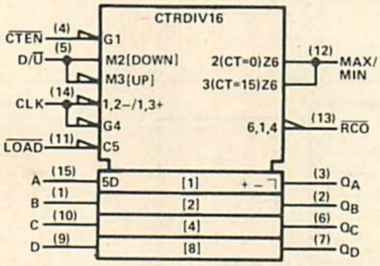
logic symbol, 'ALS190†



191

SYNCHRONOUS UP/DOWN COUNTERS (binary)

logic symbol,'191, 'LS191†



pin assignments

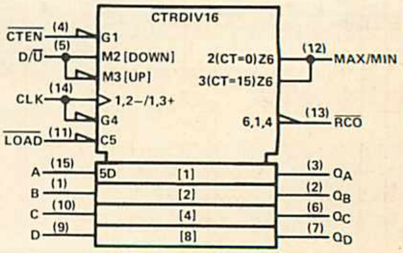
J, N PACKAGES				FH, FN PACKAGES			
1	B	9	D	1	nc	11	nc
2	Q_B	10	C	2	B	12	D
3	Q_A	11	$\overline{\text{LOAD}}$	3	Q_B	13	C
4	$\overline{\text{CTEN}}$	12	MAX/MIN	4	Q_A	14	$\overline{\text{LOAD}}$
5	D/$\overline{\text{U}}$	13	$\overline{\text{RCO}}$	5	$\overline{\text{CTEN}}$	15	MAX/MIN
6	Q_C	14	CLK	6	nc	16	nc
7	Q_D	15	A	7	D/$\overline{\text{U}}$	17	$\overline{\text{RCO}}$
8	GND	16	V_{CC}	8	Q_C	18	CLK
				9	Q_D	19	A
				10	GND	20	V_{CC}

typical performance

TYPE	COUNT FREQ	TOTAL POWER
'191	20 MHz	325 mW
'ALS191	35 MHz	60 mW
'LS191	20 MHz	90 mW

SN54191 (J,FH)	SN74191 (J,N)
SN54ALS191 (J,FH)	SN74ALS191 (N,FN)
SN54LS191 (J,FH)	SN74LS191 (J,N,FN)

logic symbol, 'ALS191†



† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

192

SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS

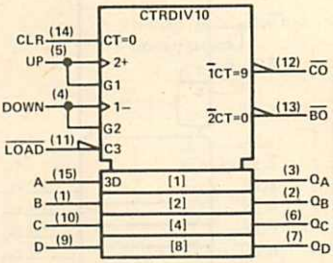
(BCD with clear)

typical performance

TYPE	COUNT FREQ	TOTAL POWER
'192	25 MHz	325 mW
'ALS192	40 MHz	50 mW
'L192	3 MHz	42 mW
'LS192	25 MHz	85 mW

SN54192 (J,FH)	SN74192 (J,N)
SN54L192 (J)	
SN54LS192 (J,FH)	SN74LS192 (J,N,FN)
SN54ALS192 (J,FH)	SN74ALS192 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	D	1	nc	11	nc
2	Q_B	10	C	2	B	12	D
3	Q_A	11	$\overline{LOAD}$	3	Q_B	13	C
4	DOWN	12	CO	4	Q_A	14	$\overline{LOAD}$
5	UP	13	$\overline{BO}$	5	DOWN	15	CO
6	Q_C	14	CLR	6	nc	16	nc
7	Q_D	15	A	7	UP	17	$\overline{BO}$
8	GND	16	V_{CC}	8	Q_C	18	CLR
				9	Q_D	19	A
				10	GND	20	V_{CC}

193

SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS

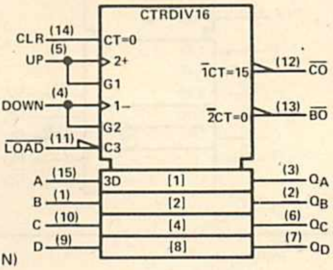
(binary with clear)

typical performance

TYPE	COUNT FREQ	TOTAL POWER
'193	25 MHz	325 mW
'ALS193	40 MHz	50 mW
'L193	3 MHz	42 mW
'LS193	25 MHz	85 mW

SN54193 (J,FH)	SN74193 (J,N)
SN54L193 (J)	
SN54LS193 (J,FH)	SN74LS193 (J,N,FN)
SN54ALS193 (J,FH)	SN74ALS193 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	D	1	nc	11	nc
2	Q_B	10	C	2	B	12	D
3	Q_A	11	$\overline{LOAD}$	3	Q_B	13	C
4	DOWN	12	$\overline{CO}$	4	Q_A	14	$\overline{LOAD}$
5	UP	13	$\overline{BO}$	5	DOWN	15	$\overline{CO}$
6	Q_C	14	CLR	6	nc	16	nc
7	Q_D	15	A	7	UP	17	$\overline{BO}$
8	GND	16	V_{CC}	8	Q_C	18	CLR
				9	Q_D	19	A
				10	GND	20	V_{CC}

194

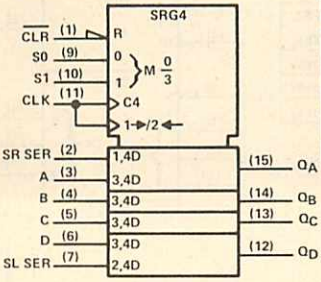
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	TOTAL POWER
'194	25 MHz	D	195 mW
'AS194			
'LS194A	25 MHz	D	75 mW
'S194	70 MHz	D	450 mW

SN54194 (J,FH)	SN74194 (J,N,FN)
SN54AS194 (J,FH)	SN74AS194 (N,FN)
SN54LS194A (J,FH)	SN74LS194A (J,N,FN)
SN54S194 (J,FH)	SN74S194 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CLR}$	9	S0	1	nc	11	nc
2	SR SER	10	S1	2	$\overline{CLR}$	12	S0
3	A	11	CLK	3	SR SER	13	S1
4	B	12	Q_D	4	A	14	CLK
5	C	13	Q_C	5	B	15	Q_D
6	D	14	Q_B	6	nc	16	nc
7	SL SER	15	Q_A	7	C	17	Q_C
8	GND	16	V_{CC}	8	D	18	Q_B
				9	SL SER	19	Q_A
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

195

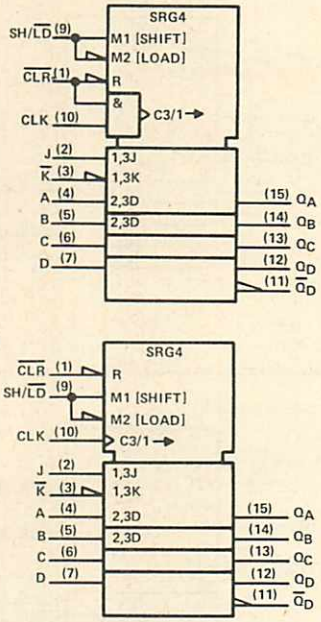
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	TOTAL POWER
'195	30 MHz	J-$\overline{\text{K}}$	195 mW
'AS195			
'LS195A	30 MHz	J-$\overline{\text{K}}$	70 mW
'S195	70 MHz	J-$\overline{\text{K}}$	375 mW

SN54195 (J,FH)	SN74195 (J,N)
SN54AS195 (J,FH)	SN74AS195 (N,FN)
SN54LS195A (J,FH)	SN74LS195A (J,N,FN)
SN54S195 (J,FH)	SN74S195 (J,N,FN)

logic symbol, '195†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{\text{CLR}}$	9	SH/$\overline{\text{LD}}$	1	nc	11	nc
2	J	10	CLK	2	$\overline{\text{CLR}}$	12	SH/$\overline{\text{LD}}$
3	$\overline{\text{K}}$	11	$\overline{Q}_D$	3	J	13	CLK
4	A	12	Q_D	4	$\overline{\text{K}}$	14	$\overline{Q}_D$
5	B	13	Q_C	5	A	15	Q_D
6	C	14	Q_B	6	nc	16	nc
7	D	15	Q_A	7	B	17	Q_C
8	GND	16	V_{CC}	8	C	18	Q_B
				9	D	19	Q_A
				10	GND	20	V_{CC}

196

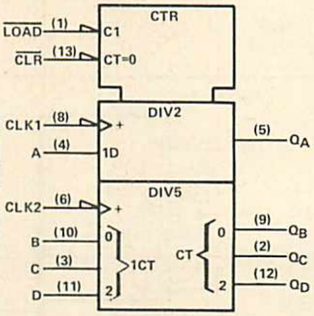
PRESETTABLE DECADE/ BIQUINARY COUNTERS/ LATCHES

typical performance

TYPE	COUNT FREQ	PARALLEL LOAD	CLEAR	TOTAL POWER
'196	50 MHz	YES	LOW	240 mW
'LS196	30 MHz	YES	LOW	60 mW
'S196	100 MHz	YES	LOW	375 mW

SN54196 (J,FH)	SN74196 (J,N)
SN54LS196 (J,FH)	SN74LS196 (J,N,FN)
SN54S196 (J,FH)	SN74S196 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{\text{LOAD}}$	8	CLK1	1	nc	11	nc
2	Q_C	9	Q_B	2	$\overline{\text{LOAD}}$	12	CLK1
3	C	10	B	3	Q_C	13	Q_B
4	A	11	D	4	C	14	B
5	Q_A	12	Q_D	5	nc	15	nc
6	CLK2	13	$\overline{\text{CLR}}$	6	A	16	D
7	GND	14	V_{CC}	7	nc	17	nc
				8	Q_A	18	Q_D
				9	CLK2	19	$\overline{\text{CLR}}$
				10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

197

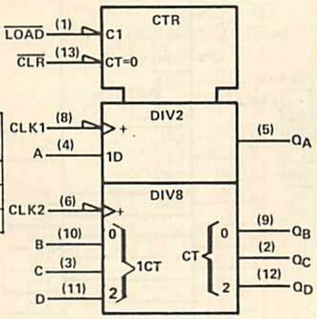
PRESETTABLE BINARY COUNTERS/LATCHES

typical performance

TYPE	COUNT FREQ	PARALLEL LOAD	CLEAR	TOTAL POWER
'197	50 MHz	YES	LOW	240 mW
'LS197	30 MHz	YES	LOW	60 mW
'S197	100 MHz	YES	LOW	375 mW

SN54197 (J,FH) SN74197 (J,N)
SN54LS197 (J,FH) SN74LS197 (J,N,FN)
SN54S197 (J,FH) SN74S197 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{\text{LOAD}}$	8	CLK1	1	nc	11	nc
2	Q_C	9	Q_B	2	$\overline{\text{LOAD}}$	12	CLK1
3	C	10	B	3	Q_C	13	Q_B
4	A	11	D	4	C	14	B
5	Q_A	12	Q_D	5	nc	15	nc
6	CLK2	13	$\overline{\text{CLR}}$	6	A	16	D
7	GND	14	V_{CC}	7	nc	17	nc
				8	Q_A	18	Q_D
				9	CLK2	19	$\overline{\text{CLR}}$
				10	GND	20	V_{CC}

198

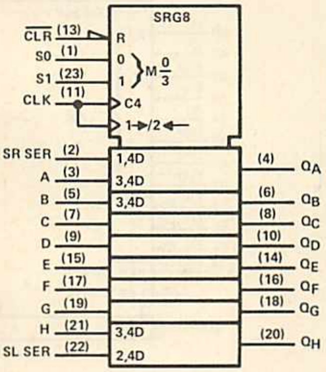
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'198	25 MHz	D	LOW	360 mW

SN54198 (J,FH) SN74198 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	S0	13	$\overline{\text{CLR}}$	1	nc	15	nc
2	SR SER	14	Q_E	2	S0	16	$\overline{\text{CLR}}$
3	A	15	E	3	SR SER	17	Q_E
4	Q_A	16	Q_F	4	A	18	E
5	B	17	F	5	Q_A	19	Q_F
6	Q_B	18	Q_G	6	B	20	F
7	C	19	G	7	Q_B	21	Q_G
8	Q_C	20	Q_H	8	nc	22	nc
9	D	21	H	9	C	23	G
10	Q_D	22	SL SER	10	Q_C	24	Q_H
11	CLK	23	S1	11	D	25	H
12	GND	24	V_{CC}	12	Q_D	26	SL SER
				13	CLK	27	S1
				14	GND	28	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

199

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

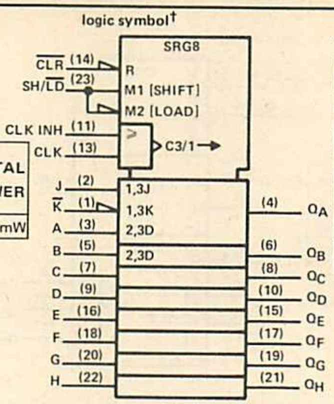
(J-$\overline{K}$ serial inputs)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'199	25 MHz	J-$\overline{K}$	LOW	360 mW

SN54199 (J,FH) SN74199 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	$\overline{K}$	13	CLK	1	nc	15	nc
2	J	14	$\overline{CLR}$	2	$\overline{K}$	16	CLK
3	A	15	Q_E	3	J	17	$\overline{CLR}$
4	Q_A	16	E	4	A	18	Q_E
5	B	17	Q_F	5	Q_A	19	E
6	Q_B	18	F	6	B	20	Q_F
7	C	19	Q_G	7	Q_B	21	F
8	Q_C	20	G	8	nc	22	nc
9	D	21	Q_H	9	C	23	Q_G
10	Q_D	22	H	10	Q_C	24	G
11	CLK INH	23	SH/$\overline{LD}$	11	D	25	Q_H
12	GND	24	V_{CC}	12	Q_D	26	H
				13	CLK INH	27	SH/$\overline{LD}$
				14	GND	28	V_{CC}

201

256-BIT RANDOM-ACCESS MEMORIES

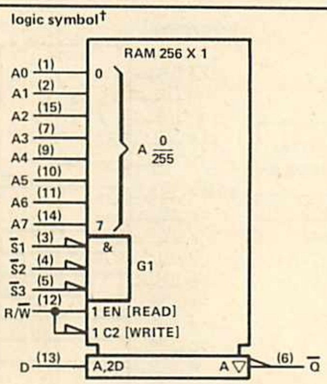
(256 1-bit words; three-state output)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'S201	42 ns	17 ns	1.9 mW

SN74S201 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	9	A4
2	A1	10	A5
3	$\overline{S}1$	11	A6
4	$\overline{S}2$	12	R/$\overline{W}$
5	$\overline{S}3$	13	D
6	$\overline{Q}$	14	A7
7	A3	15	A2
8	GND	16	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

219

64-BIT RANDOM-ACCESS MEMORIES

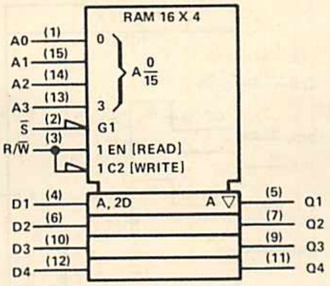
(16 words of 4 bits each; three-state non-inverting output)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'LS219A	50 ns	35 ns	2.7 mW

SN54LS219A (J,FH) SN74LS219A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A0	9	Q3	1	nc	11	nc
2	$\overline{S}$	10	D3	2	A0	12	Q3
3	R/$\overline{W}$	11	Q4	3	$\overline{S}$	13	D3
4	D1	12	D4	4	R/$\overline{W}$	14	Q4
5	Q1	13	A3	5	D1	15	D4
6	D2	14	A2	6	nc	16	nc
7	Q2	15	A1	7	Q1	17	A3
8	GND	16	V_{CC}	8	D2	18	A2
				9	Q2	19	A1
				10	GND	20	V_{CC}

221

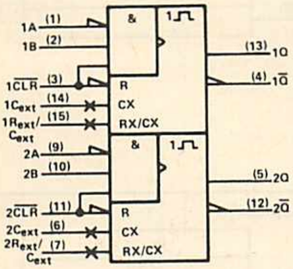
DUAL MONOSTABLE MULTIVIBRATORS

typical performance

TYPE	OUTPUT PULSE RANGE	TOTAL POWER
SN54221	20 ns - 21s	130 mW
SN74221	20 ns - 28s	130 mW
SN54LS221	20 ns - 49s	23 mW
SN74LS221	20 ns - 70 s	23 mW

SN54221 (J,FH) SN74221 (J,N)
SN54LS221 (J,FH) SN74LS221 (J,N,FN)

logic symbol†



pin assignments

J,N PACKAGES				FH, FN PACKAGES			
1	1A	9	2A	1	nc	11	nc
2	1B	10	2B	2	1A	12	2A
3	1$\overline{CLR}$	11	2$\overline{CLR}$	3	1B	13	2B
4	1$\overline{Q}$	12	2$\overline{Q}$	4	1$\overline{CLR}$	14	2$\overline{CLR}$
5	2Q	13	1Q	5	1$\overline{Q}$	15	2$\overline{Q}$
6	2C_{ext}	14	1C_{ext}	6	nc	16	nc
7	2R_{ext}/C_{ext}	15	1R_{ext}/C_{ext}	7	2Q	17	1Q
8	GND	16	V_{CC}	8	2C_{ext}	18	1C_{ext}
				9	2R_{ext}/C_{ext}	19	1R_{ext}/C_{ext}
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

222

64-BIT FIFO MEMORIES

16 4-BIT WORDS

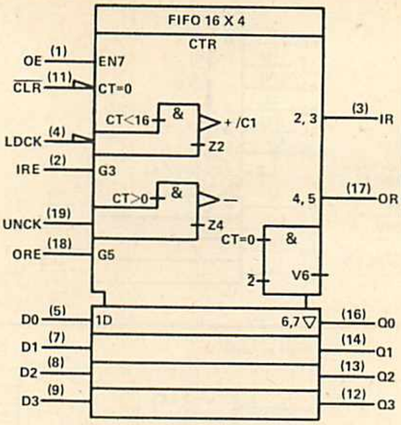
(input-ready enable, output-ready enable, and three-state output)

typical performance

TYPE	DELAY TIME FROM CLOCK	TOTAL POWER
'LS222	47 ns	433 mW

SN54LS222 (J) SN74LS222 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	OE	11	$\overline{\text{CLR}}$
2	IRE	12	Q3
3	IR	13	Q2
4	LDCK	14	Q1
5	D0	15	nc
6	nc	16	Q0
7	D1	17	OR
8	D2	18	ORE
9	D3	19	UNCK
10	GND	20	V_{CC}

For chip carrier information, contact the factory.

224

64-BIT FIFO MEMORIES

16 4-BIT WORDS

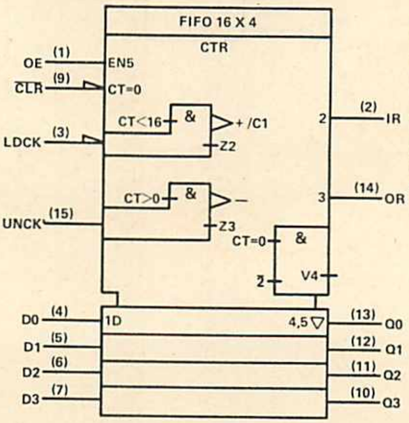
(three-state output)

typical performance

TYPE	DELAY TIME FROM CLOCK	TOTAL POWER
'LS224	47 ns	433 mW

SN54LS224 (J) SN74LS224 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	OE	9	$\overline{\text{CLR}}$
2	IR	10	Q3
3	LDCK	11	Q2
4	D0	12	Q1
5	D1	13	Q0
6	D2	14	OR
7	D3	15	UNCK
8	GND	16	V_{CC}

For chip carrier information, contact the factory.

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

225

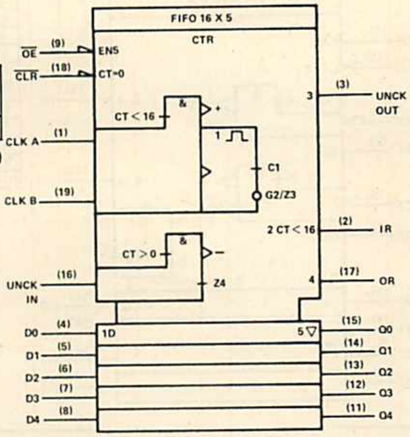
80-BIT FIFO MEMORIES
16 5-BIT WORDS

typical performance

OUTPUT	DELAY TIME FROM CLOCK	TOTAL POWER
3-State	50 ns	400 mW

SN74S225 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	CLK A	11	Q4
2	IR	12	Q3
3	UNCK OUT	13	Q2
4	D0	14	Q1
5	D1	15	Q0
6	D2	16	UNCK IN
7	D3	17	OR
8	D4	18	$\overline{\text{CLR}}$
9	$\overline{\text{OE}}$	19	CLK B
10	GND	20	V_{CC}

FN PACKAGES			
1	CLK A	11	Q4
2	IR	12	Q3
3	UNCK OUT	13	Q2
4	D0	14	Q1
5	D1	15	Q0
6	D2	16	UNCK IN
7	D3	17	OR
8	D4	18	$\overline{\text{CLR}}$
9	$\overline{\text{OE}}$	19	CLK B
10	GND	20	V_{CC}

226

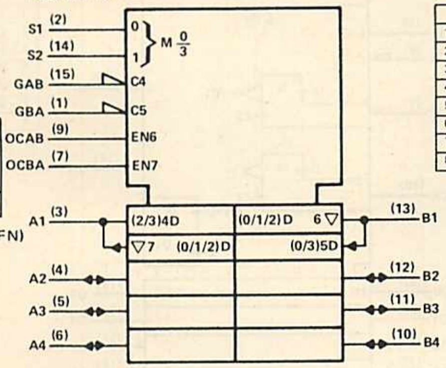
4-BIT PARALLEL LATCHED BUS TRANSCEIVERS
(three-state outputs)

typical performance

TYPE	MAX SOURCE CURRENT	MAX SINK CURRENT
'S226	−6.5 mA	20 mA

SN54S226 (J,FH) SN74S226 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	GBA	9	OCAB	1	nc	11	nc
2	S1	10	B4	2	GBA	12	OCAB
3	A1	11	B3	3	S1	13	B4
4	A2	12	B2	4	A1	14	B3
5	A3	13	B1	5	A2	15	B2
6	A4	14	S2	6	nc	16	nc
7	OCBA	15	GAB	7	A3	17	B1
8	GND	16	V_{CC}	8	A4	18	S2
				9	OCBA	19	GAB
				10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

227

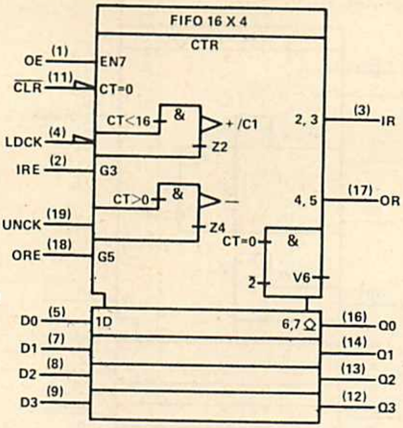
64-BIT FIFO MEMORIES
16 4-BIT WORDS
(input-ready enable, output-ready enable, open-collector outputs)

typical performance

TYPE	DELAY TIME FROM CLOCK	TOTAL POWER
'LS227	57.5 ns	433 mW

SN54LS227 (J)   SN74LS227 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	OE	11	$\overline{\text{CLR}}$
2	IRE	12	Q3
3	IR	13	Q2
4	LDCK	14	Q1
5	D0	15	nc
6	nc	16	Q0
7	D1	17	OR
8	D2	18	ORE
9	D3	19	UNCK
10	GND	20	V_{CC}

For chip carrier information, contact the factory.

228

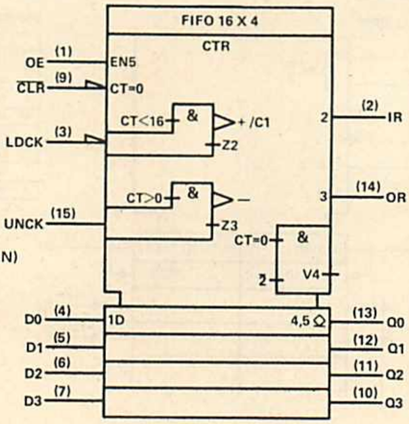
64-BIT FIFO MEMORIES
16 4-BIT WORDS
(open-collector outputs)

typical performance

TYPE	DELAY TIME FROM CLOCK	TOTAL POWER
'LS228	57.5 ns	433 mW

SN54LS228 (J)   SN74LS228 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	OE	9	$\overline{\text{CLR}}$
2	IR	10	Q3
3	LDCK	11	Q2
4	D0	12	Q1
5	D1	13	Q0
6	D2	14	OR
7	D3	15	UNCK
8	GND	16	V_{CC}

For chip carrier information, contact the factory.

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

230,231

OCTAL BUFFERS AND LINE DRIVERS

(three-state outputs)

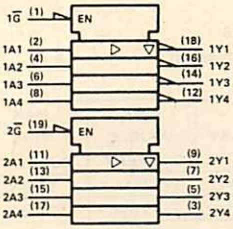
- 'AS230 has true and complementary outputs
- 'AS231 has complementary G and G̅ inputs

typical performance

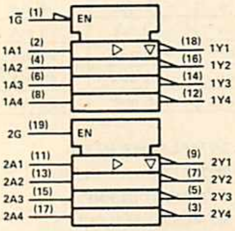
DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
3.5 ns	−15 mA	64 mA

SN54AS230 (J,FH) SN74AS230 (N,FN)
SN54AS231 (J,FH) SN74AS231 (N,FN)

logic symbol, 'AS230†



logic symbol, 'AS231†



pin assignments

J, N PACKAGES			
1	1G̅	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2G̅
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1G̅	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2G̅
10	GND	20	V_{CC}

*2G on 'AS231

240

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

(inverted three-state outputs)

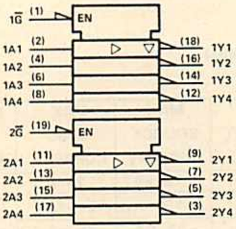
typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSI-PATION
SN54ALS240A	5.5 ns	−12 mA	12 mA	52 mW
SN74ALS240A	5.5 ns	−15 mA	24 mA	
SN74ALS240A-1	5.5 ns	−15 mA	48 mA	
SN54AS240	3.5 ns	−12 mA	48 mA	235 mW
SN74AS240	3.5 ns	−15 mA	64 mA	
SN54LS240	10 ns	−12 mA	12 mA	120 mW
SN74LS240	10 ns	−15 mA	24 mA	
SN54S240	5 ns	−12 mA	48 mA	467 mW
SN74S240	5 ns	−15 mA	64 mA	

SN54ALS240A (J,FH) SN74ALS240A (N,FN)
SN74ALS240A-1 (N,FN)

SN54AS240 (J,FH) SN74AS240 (N,FN)
SN54LS240 (J,FH) SN74LS240 (J,N,FN)
SN54S240 (J,FH) SN74S240 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1G̅	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2G̅
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1G̅	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2G̅
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

241

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

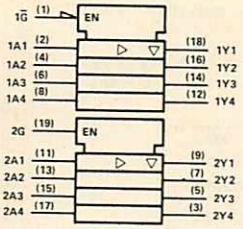
(non-inverted three-state outputs)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSI-PATION
SN54ALS241A	7 ns	−12 mA	12 mA	68 mW
SN74ALS241A	7 ns	−15 mA	24 mA	
SN74ALS241A-1	7 ns	−15 mA	48 mA	
SN54AS241	4 ns	−12 mA	48 mA	195 mW
SN74AS241	4 ns	−15 mA	64 mA	
SN54LS241	10 ns	−12 mA	12 mA	127 mW
SN74LS241	10 ns	−15 mA	24 mA	
SN54S241	5 ns	−12 mA	48 mA	558 mW
SN74S241	5 ns	−15 mA	64 mA	

SN54ALS241A (J,FH)	SN74ALS241A (N,FN)
	SN74ALS241A-1 (N,FN)
SN54AS241 (J,FH)	SN74AS241 (N,FN)
SN54LS241 (J,FH)	SN74LS241 (J,N,FN)
SN54S241 (J,FH)	SN74S241 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1$\overline{\text{G}}$	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2G
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1$\overline{\text{G}}$	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2G
10	GND	20	V_{CC}

242

QUADRUPLE BUS TRANSCEIVERS

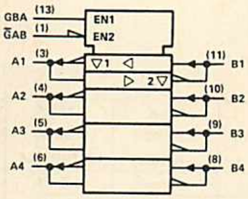
(inverted three-state outputs)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSI-PATION
SN54ALS242A	6 ns	−12 mA	12 mA	68 mW
SN74ALS242A	6 ns	−15 mA	24 mA	
SN74ALS242A-1	6 ns	−15 mA	48 mA	
SN54AS242	3.5 ns	−12 mA	48 mA	135 mW
SN74AS242	3.5 ns	−15 mA	64 mA	
SN54LS242	11 ns	−12 mA	12 mA	133 mW
SN74LS242	11 ns	−15 mA	24 mA	

SN54ALS242A (J, FH)	SN74ALS242A (N, FN)
	SN74ALS242A-1 (N, FN)
SN54AS242 (J,FH)	SN74AS242 (N,FN)
SN54LS242 (J,FH)	SN74LS242 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{\text{G}}$AB	8	B4
2	nc	9	B3
3	A1	10	B2
4	A2	11	B1
5	A3	12	nc
6	A4	13	GBA
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	$\overline{\text{G}}$AB	12	B4
3	nc	13	B3
4	A1	14	B2
5	nc	15	nc
6	A2	16	B1
7	nc	17	nc
8	A3	18	nc
9	A4	19	GBA
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

243

QUADRUPLE BUS TRANSCEIVERS

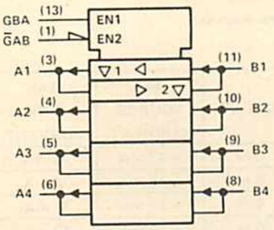
(non-inverted three-state outputs)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSI-PATION
SN54ALS243A	8 ns	−12 mA	12 mA	93 mW
SN74ALS243A	8 ns	−15 mA	24 mA	
SN74ALS243A-1	8 ns	−15 mA	48 mA	
SN54AS243	4.5 ns	−12 mA	48 mA	180 mW
SN74AS243	4.5 ns	−15 mA	64 mA	
SN54LS243	12 ns	−12 mA	12 mA	138 mW
SN74LS243	12 ns	−15 mA	24 mA	

SN54ALS243A (J,FH)	SN74ALS243A (N,FN) SN74ALS243A-1 (N,FN)
SN54AS243 (J,FH)	SN74AS243 (N,FN)
SN54LS243 (J,FH)	SN74LS243 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{G}$AB	8	B4
2	nc	9	B3
3	A1	10	B2
4	A2	11	B1
5	A3	12	nc
6	A4	13	GBA
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	$\overline{G}$AB	12	B4
3	nc	13	B3
4	A1	14	B2
5	nc	15	nc
6	A2	16	B1
7	nc	17	nc
8	A3	18	nc
9	A4	19	GBA
10	GND	20	V_{CC}

244

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

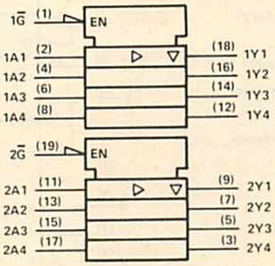
(non-inverted three-state outputs)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSI-PATION
SN54ALS244A	7 ns	− 12 mA	12 mA	68 mW
SN74ALS244A	7 ns	− 15 mA	24 mA	
SN74ALS244A-1	7 ns	− 15 mA	48 mA	
SN54AS244	4.5 ns	− 12 mA	48 mA	235 mW
SN74AS244	4.5 ns	− 15 mA	64 mA	
SN54LS244	12 ns	− 12 mA	12 mA	127 mW
SN74LS244	12 ns	− 15 mA	24 mA	
SN54S244	6 ns	− 12 mA	48 mA	558 mW
SN74S244	6 ns	− 15 mA	64 mA	

SN54ALS244A (J,FH)	SN74ALS244A (N,FN) SNALS244A-1 (N,FN)
SN54AS244 (J,FH)	SN74AS244 (N,FN)
SN54LS244 (J,FH)	SN74LS244 (J,N,FN)
SN54S244 (J,FH)	SN74S244 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1$\overline{G}$	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2$\overline{G}$
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1$\overline{G}$	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	2$\overline{G}$
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

245

OCTAL BUS TRANSCEIVERS

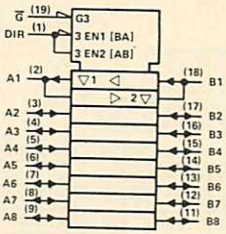
(non-inverted three-state outputs)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSI-PATION
SN54ALS245A	6 ns	−12 mA	12 mA	173 mW
SN74ALS245A	6 ns	−15 mA	24 mA	
SN74ALS245A-1	6 ns	−15 mA	48 mA	
SN54AS245	6 ns	−12 mA	32 mA	310 mW
SN74AS245	6 ns	−15 mA	48 mA	
SN54LS245	8 ns	−12 mA	12 mA	290 mW
SN74LS245	8 ns	−15 mA	24 mA	

SN54ALS245A (J,FH)
SN74ALS245A (N,FN)
SN74ALS245A-1 (N,FN)
SN54AS245 (J,FH)
SN74AS245 (N,FN)
SN54LS245 (J,FH)
SN74LS245 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{G}$
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	G
10	GND	20	V_{CC}

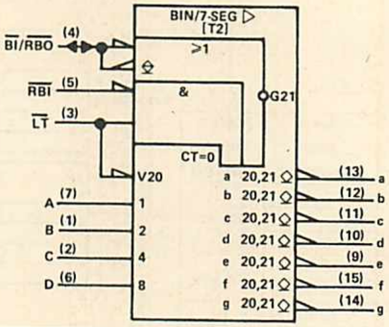
246
247

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS WITH RIPPLE BLANKING

(246-active-low, open-collector, 30-volt outputs)

(247-active-low, open-collector, 15-volt outputs)

logic symbol†



pin assignments

J, N PACKAGES			
1	B	9	e
2	C	10	d
3	$\overline{LT}$	11	c
4	$\overline{BI}/\overline{RBO}$	12	b
5	$\overline{RBI}$	13	a
6	D	14	g
7	A	15	f
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	B	12	e
3	C	13	d
4	$\overline{LT}$	14	c
5	$\overline{BI}/\overline{RBO}$	15	b
6	nc	16	nc
7	RBI	17	a
8	D	18	g
9	A	19	f
10	GND	20	V_{CC}

typical performance

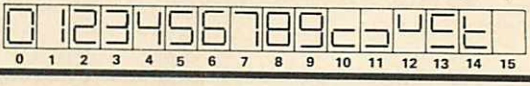
TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'246	40 mA	30 V	320 mW
'247	40 mA	15 V	320 mW
SN54LS247	12 mA	15 V	35 mW
SN74LS247	24 mA	15 V	35 mW

SN54246 (J,FH)
SN74246 (J,N)
SN54247 (J,FH)
SN74247 (J,N)
SN54LS247 (J,FH)
SN74LS247 (J,N,FN)

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

FONT TABLE T2 – RESULTANT DISPLAYS USING '246 AND '247

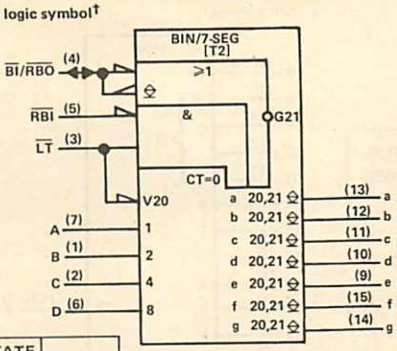


248

BCD-TO-SEVEN SEGMENT DECODERS/DRIVERS

(internal pull-up outputs)

logic symbol†



pin assignments

J, N PACKAGES			
1	B	9	e
2	C	10	d
3	$\overline{LT}$	11	c
4	$\overline{BI}/\overline{RBO}$	12	b
5	$\overline{RBI}$	13	a
6	D	14	g
7	A	15	f
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	B	12	e
3	C	13	d
4	$\overline{LT}$	14	c
5	$\overline{BI}/\overline{RBO}$	15	b
6	nc	16	nc
7	$\overline{RBI}$	17	a
8	D	18	g
9	A	19	f
10	GND	20	V_{CC}

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'248	6.4 mA	5.5 V	265 mW
SN54LS248	2 mA	5.5 V	125 mW
SN74LS248	6 mA	5.5 V	125 mW

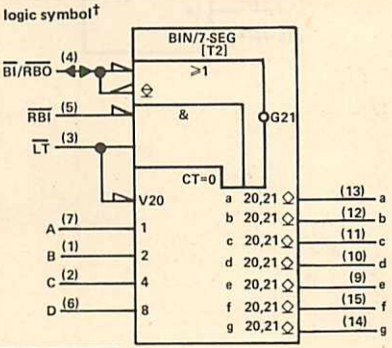
SN54248 (J,FH) SN74248 (J,N)
SN54LS248 (J,FH) SN74LS248 (J,N,FN)

249

BCD-TO-SEVEN SEGMENT DECODERS/DRIVERS

(open-collector outputs)

logic symbol†



pin assignments

J, N PACKAGES			
1	B	9	e
2	C	10	d
3	$\overline{LT}$	11	c
4	$\overline{BI}/\overline{RBO}$	12	b
5	$\overline{RBI}$	13	a
6	D	14	g
7	A	15	f
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	B	12	e
3	C	13	d
4	$\overline{LT}$	14	c
5	$\overline{BI}/\overline{RBO}$	15	b
6	nc	16	nc
7	$\overline{RBI}$	17	a
8	D	18	g
9	A	19	f
10	GND	20	V_{CC}

typical performance

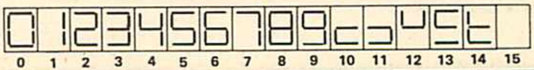
TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
'249	10 mA	5.5 V	265 mW
SN54LS249	4 mA	5.5 V	40 mW
SN74LS249	8 mA	5.5 V	40 mW

SN54249 (J,FH) SN74249 (J,N)
SN54LS249 (J,FH) SN74LS249 (J,N,FN)

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

FONT TABLE T2 — RESULTANT DISPLAYS USING '248 AND '249



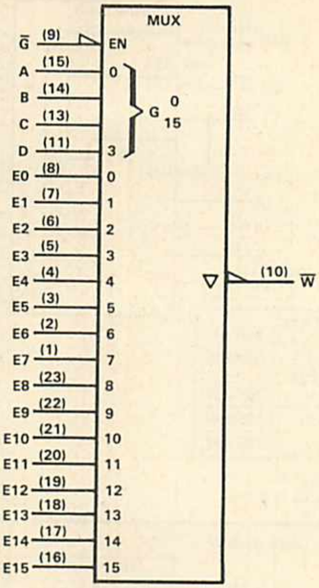
250

1-OF-16 DATA SELECTORS/ MULTIPLEXERS

TYPE	DATA TO INV OUTPUT	FROM ENABLE	TOTAL POWER
'AS250			

SN54AS250 (J,FH) SN74AS250 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	E7	13	C
2	E6	14	B
3	E5	15	A
4	E4	16	E15
5	E3	17	E14
6	E2	18	E13
7	E1	19	E12
8	E0	20	E11
9	G̅	21	E10
10	W̅	22	E9
11	D	23	E8
12	GND	24	V_{CC}

FH PACKAGE			
1	NC	15	NC
2	E7	16	C
3	E6	17	B
4	E5	18	A
5	E4	19	E15
6	E3	20	E14
7	E2	21	E13
8	NC	22	NC
9	E1	23	E12
10	E0	24	E11
11	G̅	25	E10
12	W̅	26	E9
13	D	27	E8
14	GND	28	V_{CC}

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†Pin numbers shown on logic symbols are for J and N packages only.

NC — No internal connection.

251

DATA SELECTORS/ MULTIPLEXERS

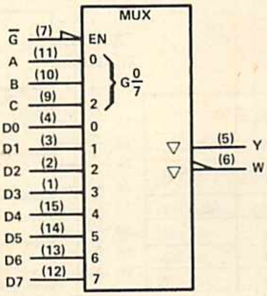
(true and inverted three-state outputs)

typical performance

TYPE	DELAY TIMES			TOTAL POWER
	DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE	
'251	17 ns	21 ns	21 ns	250 mW
'ALS251	6 ns	5 ns	4.5 ns	37.5 mW
'AS251	2.7 ns	3.5 ns	5.5 ns	140 mW
'LS251	17 ns	21 ns	21 ns	35 mW
'S251	4.5 ns	8 ns	14 ns	275 mW

SN54251 (J,FH)	SN74251 (J,N)
SN54ALS251 (J,FH)	SN74ALS251 (N,FN)
SN54AS251 (J,FH)	SN74AS251 (N,FN)
SN54LS251 (J,FH)	SN74LS251 (J,N,FN)
SN54S251 (J,FH)	SN74S251 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	D3	9	C
2	D2	10	B
3	D1	11	A
4	D0	12	D7
5	Y	13	D6
6	W	14	D5
7	$\overline{G}$	15	D4
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	D3	12	C
3	D2	13	B
4	D1	14	A
5	D0	15	D7
6	nc	16	nc
7	Y	17	D6
8	W	18	D5
9	$\overline{G}$	19	D4
10	GND	20	V_{CC}

253

DUAL DATA SELECTORS/ MULTIPLEXERS

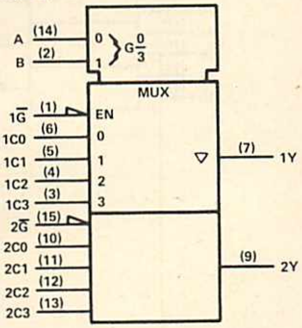
(three-state outputs)

typical performance

TYPE	DELAY TIMES		TOTAL POWER
	DATA TO NON-INV OUTPUT	FROM ENABLE	
'ALS253	5 ns	4.5 ns	32 mW
'AS253	3.3 ns	5.5 ns	117 mW
'LS253	12 ns	16 ns	35 mW

SN54ALS253 (J,FH)	SN74ALS253 (N,FN)
SN54AS253 (J,FH)	SN74AS253 (N,FN)
SN54LS253 (J,FH)	SN74LS253 (J,N,FN)
SN54S253 (J,FH)	SN74S253 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$1\overline{G}$	9	2Y
2	B	10	2C0
3	1C3	11	2C1
4	1C2	12	2C2
5	1C1	13	2C3
6	1C0	14	A
7	1Y	15	$2\overline{G}$
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	$1\overline{G}$	12	2Y
3	B	13	2C0
4	1C3	14	2C1
5	1C2	15	2C2
6	nc	16	nc
7	1C1	17	2C3
8	1C0	18	A
9	1Y	19	$2\overline{G}$
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

257

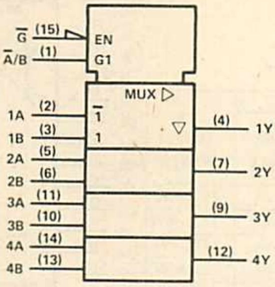
QUAD DATA SELECTORS/ MULTIPLEXERS

(non-inverted three-state outputs)

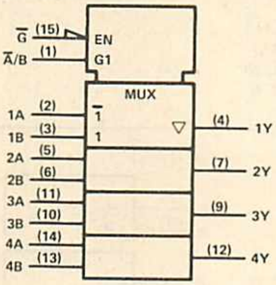
TYPE	DELAY TIMES		TOTAL POWER
	DATA TO NON-INV OUTPUT	FROM ENABLE	
'ALS257	4.3 ns	7.5 ns	33.5 mW
'AS257	3 ns	4 ns	85 mW
'LS257B	11 ns	18 ns	60 mW
'S257	5 ns	14 ns	320 mW

SN54ALS257 (J,FH)	SN74ALS257 (N,FN)
SN54AS257 (J,FH)	SN74AS257 (N,FN)
SN54ALS257B (J,FH)	SN74ALS257B (J,N,FN)
SN54S257 (J,FH)	SN74S257 (J,N,FN)

logic symbol, 'ALS257, 'LS257†



logic symbol, 'S257†



pin assignments

J, N PACKAGES			
1	$\overline{A}$/B	9	3Y
2	1A	10	3B
3	1B	11	3A
4	1Y	12	4Y
5	2A	13	4B
6	2B	14	4A
7	2Y	15	$\overline{G}$
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	$\overline{A}$/B	12	3Y
3	1A	13	3B
4	1B	14	3A
5	1Y	15	4Y
6	nc	16	nc
7	2A	17	4B
8	2B	18	4A
9	2Y	19	$\overline{G}$
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

258

QUAD DATA SELECTORS/ MULTIPLEXERS

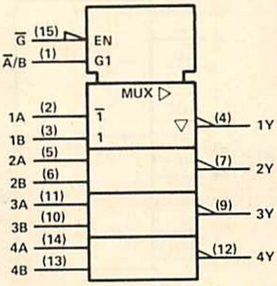
(inverted three-state outputs)

typical performance

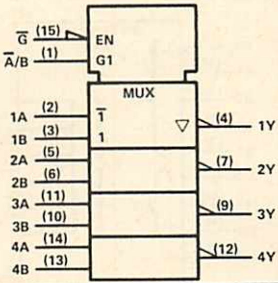
TYPE	DELAY TIMES		TOTAL POWER
	DATA TO INV OUTPUT	FROM ENABLE	
'ALS258	3 ns	7.5 ns	29 mW
'AS258	2.5 ns	4 ns	65 mW
'LS258B	11 ns	19 ns	60 mW
'S258	4 ns	14 ns	280 mW

SN54ALS258 (J,FH)	SN74ALS258 (N,FN)
SN54AS258 (J,FH)	SN74AS258 (N,FN)
SN54LS258B (J,FH)	SN74LS258B (J,N,FN)
SN54S258 (J,FH)	SN74S258 (J,N,FN)

logic symbol, 'ALS258, 'LS258†



logic symbol, 'S258†



pin assignments

J, N PACKAGES			
1	$\overline{\mathrm{A}}$/B	9	3Y
2	1A	10	3B
3	1B	11	3A
4	1Y	12	4Y
5	2A	13	4B
6	2B	14	4A
7	2Y	15	$\overline{\mathrm{G}}$
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	$\overline{\mathrm{A}}$/B	12	3Y
3	1A	13	3B
4	1B	14	3A
5	1Y	15	4Y
6	nc	16	nc
7	2A	17	4B
8	2B	18	4A
9	2Y	19	$\overline{\mathrm{G}}$
10	GND	20	V_{CC}

259

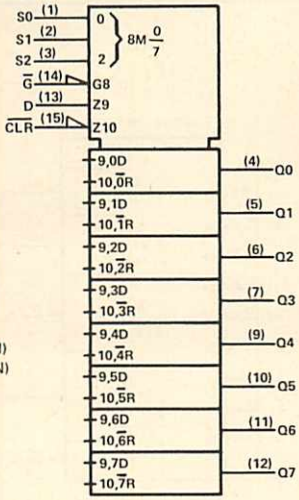
8-BIT ADDRESSABLE LATCHES

typical performance

TYPE	CLEAR	DELAY	TOTAL POWER
'259	LOW	12 ns	300 mW
'ALS259	LOW		
'LS259	LOW	17 ns	110 mW

SN54259 (J,FH)	SN74259 (J,N)
SN54ALS259 (J,FH)	SN74ALS259 (N,FN)
SN54LS259 (J,FH)	SN74LS259 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	S0	9	Q4
2	S1	10	Q5
3	S2	11	Q6
4	Q0	12	Q7
5	Q1	13	D
6	Q2	14	$\overline{\mathrm{G}}$
7	Q3	15	$\overline{\mathrm{CLR}}$
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	S0	12	Q4
3	S1	13	Q5
4	S2	14	Q6
5	Q0	15	Q7
6	nc	16	nc
7	Q1	17	D
8	Q2	18	$\overline{\mathrm{G}}$
9	Q3	19	$\overline{\mathrm{CLR}}$
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

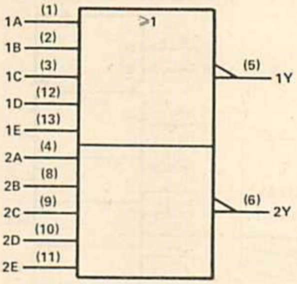
260

DUAL 5-INPUT POSITIVE-NOR GATES

TYPE	POWER/ GATE	DELAY
'S260	54 mW	4 ns

SN54S260 (J,FH) SN74S260 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	2B	1	nc	11	nc
2	1B	9	2C	2	1A	12	2B
3	1C	10	2D	3	1B	13	2C
4	2A	11	2E	4	1C	14	2D
5	1Y	12	1D	5	nc	15	nc
6	2Y	13	1E	6	2A	16	2E
7	GND	14	V_{CC}	7	nc	17	nc
				8	1Y	18	1D
				9	2Y	19	1E
				10	GND	20	V_{CC}

positive logic: $Y = \overline{ABCD}$

261

2-BIT BY 4-BIT PARALLEL BINARY MULTIPLIERS

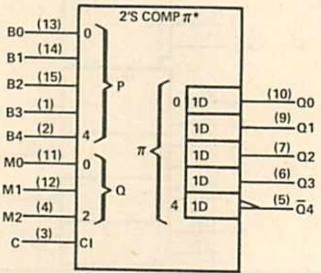
typical performance

TYPE	POWER	TIME**
'LS261	100 mW	25 ns

SN54LS261 (J,FH) SN74LS261 (J,N,FN)

** 5-Bit Product Time

logic symbol†



* Partial-Product Generator

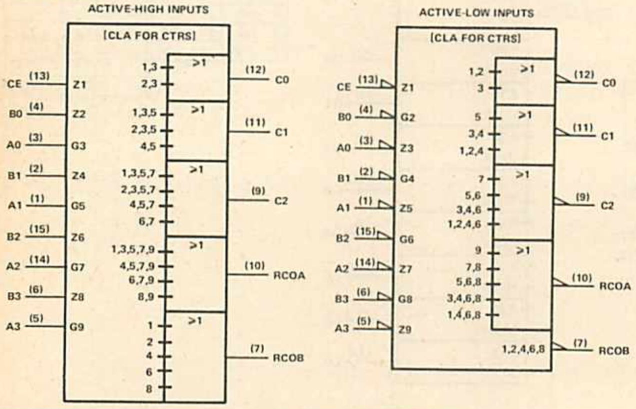
pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B3	9	Q1	1	nc	11	nc
2	B4	10	Q0	2	B3	12	Q1
3	C	11	M0	3	B4	13	Q0
4	M2	12	M1	4	C	14	M0
5	$\overline{Q4}$	13	B0	5	M2	15	M1
6	Q3	14	B1	6	nc	16	nc
7	Q2	15	B2	7	$\overline{Q4}$	17	B0
8	GND	16	V_{CC}	8	Q3	18	B1
				9	Q2	19	B2
				10	GND	20	V_{CC}

264

LOOK AHEAD CARRY GENERATOR

logic symbol†



ACTIVE-HIGH INPUTS

ACTIVE-LOW INPUTS

pin assignments

J, N PACKAGES				FH PACKAGES			
1	A1	9	C2	1	NC	11	NC
2	B1	10	RCOA	2	A1	12	C2
3	a0	11	C1	3	B1	13	RCOA
4	B0	12	C0	4	A0	14	C1
5	A3	13	CE	5	B0	15	C0
6	B3	14	A2	6	NC	16	NC
7	RCOB	15	B2	7	A3	17	CE
8	GND	16	V_{CC}	8	B3	18	A2
				9	RCOB	19	B2
				10	GND	20	V_{CC}

SN54AS264 (J,FH) SN74AS264 (N,FN)

For further information, contact the factory.

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† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

265

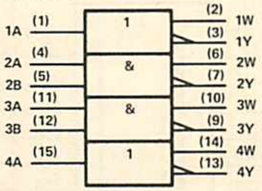
QUAD COMPLEMENTARY-OUTPUT ELEMENTS

typical performance

TYPE	POWER
'265	125 mW

SN54265 (J,FH) SN74265 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	1A	9	3Y	1	nc	11	nc
2	1W	10	3W	2	1A	12	3Y
3	1Y	11	3A	3	1W	13	3W
4	2A	12	3B	4	1Y	14	3A
5	2B	13	4Y	5	2A	15	3B
6	2W	14	4W	6	nc	16	nc
7	2Y	15	4A	7	2B	17	4Y
8	GND	16	V_{CC}	8	2W	18	4W
				9	2Y	19	4A
				10	GND	20	V_{CC}

266

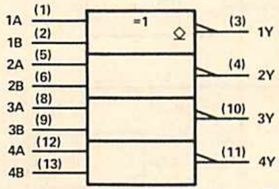
QUAD 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

typical performance

TYPE	POWER	DELAY
'LS266	40 mW	18 ns

SN54LS266 (J,FH) SN74LS266 (J,N,FN)

logic symbol†



positive logic: $Y = \overline{A \oplus B} = AB + \overline{A}\overline{B}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3A	1	nc	11	nc
2	1B	9	3B	2	1A	12	3A
3	1Y	10	3Y	3	1B	13	3B
4	2Y	11	4Y	4	1Y	14	3Y
5	2A	12	4A	5	nc	15	nc
6	2B	13	4B	6	2Y	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4A
				9	2B	19	4B
				10	GND	20	V_{CC}

268

HEX D-TYPE LATCHES

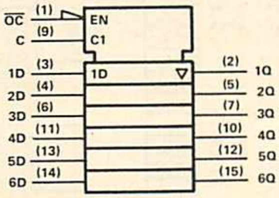
(three-state outputs, common output control, common enable)

typical performance

TYPE	OUT-PUTS	DELAY	TOTAL POWER
'S268	Q	7 ns	525 mW

SN54S268 (J,FH) SN74S268 (J,N,FN)

logic symbol



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{\text{OC}}$	9	C	1	NC	11	NC
2	1Q	10	4Q	2	$\overline{\text{OC}}$	12	C
3	1D	11	4D	3	1Q	13	4Q
4	2D	12	5Q	4	1D	14	4D
5	2Q	13	5D	5	2D	15	5Q
6	3D	14	6D	6	NC	16	NC
7	3Q	15	6Q	7	2Q	17	5D
8	GND	16	V_{CC}	8	3D	18	6D
				9	3Q	19	6Q
				10	GND	20	V_{CC}

273

OCTAL D-TYPE FLIP-FLOPS

(common clock, single-rail outputs)

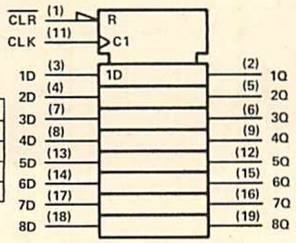
typical performance

TYPE	FREQ	POWER PER F-F	DATA TIMES	
			SETUP	HOLD
'273	40 MHz	39 mW	20 ns↑	5 ns↑
'ALS273	50 MHz	9.4 mW		
'LS273	40 MHz	10.6 mW	20 ns↑	5 ns↑

↑ Rising edge of clock pulse

SN54273 (J,FH) SN74273 (J,N)
SN54ALS273 (J,FH) SN74ALS273 (N,FN)
SN54LS273 (J,FH) SN74LS273 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{\text{CLR}}$	11	CLK	1	$\overline{\text{CLR}}$	11	CLK
2	1Q	12	5Q	2	1Q	12	5Q
3	1D	13	5D	3	1D	13	5D
4	2D	14	6D	4	2D	14	6D
5	2Q	15	6Q	5	2Q	15	6Q
6	3Q	16	7Q	6	3Q	16	7Q
7	3D	17	7D	7	3D	17	7D
8	4D	18	8D	8	4D	18	8D
9	4Q	19	8Q	9	4Q	19	8Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

274

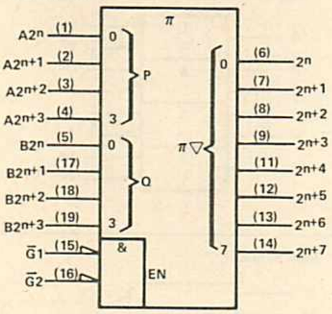
4-BIT BY 4-BIT BINARY MULTIPLIERS

typical performance

TYPE	POWER	TIME*
'S274	525 mW	50 ns

SN54S274 (J,FH) SN74S274 (J,N,FN)

logic symbol†



pin assignments

J. N PACKAGES				FH, FN PACKAGES			
1	$A2^{n}$	11	2^{n+4}	1	$A2^{n}$	11	2^{n+4}
2	$A2^{n+1}$	12	2^{n+5}	2	$A2^{n+1}$	12	2^{n+5}
3	$A2^{n+2}$	13	2^{n+6}	3	$A2^{n+2}$	13	2^{n+6}
4	$A2^{n+3}$	14	2^{n+7}	4	$A2^{n+3}$	14	2^{n+7}
5	$B2^{n}$	15	$\overline{G}1$	5	$B2^{n}$	15	$\overline{G}1$
6	2^{n}	16	$\overline{G}2$	6	2^{n}	16	$\overline{G}2$
7	2^{n+1}	17	$B2^{n+1}$	7	2^{n+1}	17	$B2^{n+1}$
8	2^{n+2}	18	$B2^{n+2}$	8	2^{n+2}	18	$B2^{n+2}$
9	2^{n+3}	19	$B2^{n+3}$	9	2^{n+3}	19	$B2^{n+3}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

* 8-Bit Product Time

276

QUAD J-K̅ FLIP-FLOPS

(separate clocks, edge-triggering, common direct clear and preset)

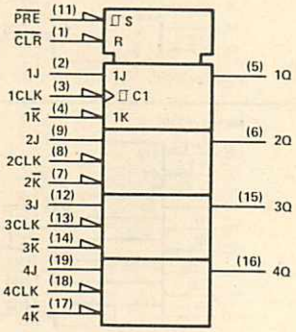
typical performance

TYPE	FREQ	POWER/ F-F	DATA TIMES	
			SETUP	HOLD
'276	50 MHz	75 mW	3 ns↓	10 ns↓

↓ Falling edge of clock pulse

SN54276 (J,FH) SN74276 (J,N)

logic symbol†



pin assignments

J. N PACKAGES				FH PACKAGE			
1	$\overline{CLR}$	11	$\overline{PRE}$	1	$\overline{CLR}$	11	$\overline{PRE}$
2	1J	12	3J	2	1J	12	3J
3	1CLK	13	3CLK	3	1CLK	13	3CLK
4	$1\overline{K}$	14	$3\overline{K}$	4	$1\overline{K}$	14	$3\overline{K}$
5	1Q	15	3Q	5	1Q	15	3Q
6	2Q	16	4Q	6	2Q	16	4Q
7	$2\overline{K}$	17	$4\overline{K}$	7	$2\overline{K}$	17	$4\overline{K}$
8	2CLK	18	4CLK	8	2CLK	18	4CLK
9	2J	19	4J	9	2J	19	4J
10	GND	20	V_{CC}	10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

278

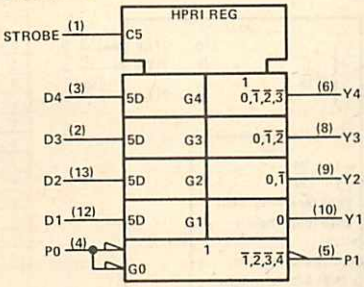
4-BIT CASCADABLE PRIORITY REGISTERS

typical performance

TYPE	POWER	DELAY
'278	275 mW	35 ns

SN54278 (J,FH) SN74278 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	STRB	8	Y3	1	nc	11	nc
2	D3	9	Y2	2	STRB	12	Y3
3	D4	10	Y1	3	D3	13	Y2
4	P0	11	nc	4	D4	14	Y1
5	P1	12	D1	5	nc	15	nc
6	Y4	13	D2	6	P0	16	nc
7	GND	14	V_{CC}	7	nc	17	nc
				8	P1	18	D1
				9	Y4	19	D2
				10	GND	20	V_{CC}

279

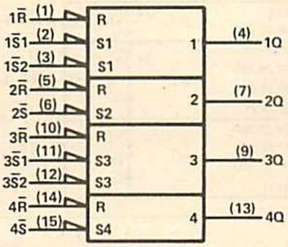
QUAD $\overline{S}$-$\overline{R}$ LATCHES

typical performance

TYPE	POWER	DELAY
'279	90 mW	12 ns
'LS279A	19 mW	12 ns

SN54279 (J,FH) SN74279 (J,N,FN)
SN54LS279A (J,FH) SN74LS279A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1$\overline{R}$	9	3Q	1	nc	11	nc
2	1$\overline{S}$1	10	3$\overline{R}$	2	1$\overline{R}$	12	3Q
3	1$\overline{S}$2	11	3$\overline{S}$1	3	1$\overline{S}$1	13	3$\overline{R}$
4	1Q	12	3$\overline{S}$2	4	1$\overline{S}$2	14	3$\overline{S}$1
5	2$\overline{R}$	13	4Q	5	1Q	15	3$\overline{S}$2
6	2$\overline{S}$	14	4$\overline{R}$	6	nc	16	nc
7	2Q	15	4$\overline{S}$	7	2$\overline{R}$	17	4Q
8	GND	16	V_{CC}	8	2$\overline{S}$	18	4$\overline{R}$
				9	2Q	19	4$\overline{S}$
				10	GND	20	V_{CC}

280

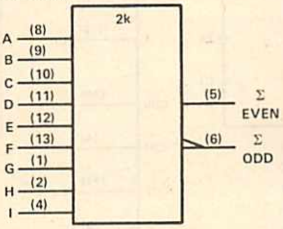
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

typical performance

TYPE	POWER	DELAY
'AS280		
'LS280	80 mW	31 ns
'S280	335 mW	13 ns

SN54AS280 (J,FH) SN74AS280 (N,FN)
SN54LS280 (J,FH) SN74LS280 (J,N,FN)
SN54S280 (J,FH) SN74S280 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	G	8	A	1	nc	11	nc
2	H	9	B	2	G	12	A
3	nc	10	C	3	H	13	B
4	I	11	D	4	nc	14	C
5	ΣEVEN	12	E	5	nc	15	nc
6	ΣODD	13	F	6	I	16	D
7	GND	14	V_{CC}	7	nc	17	nc
				8	ΣEVEN	18	E
				9	ΣODD	19	F
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

281

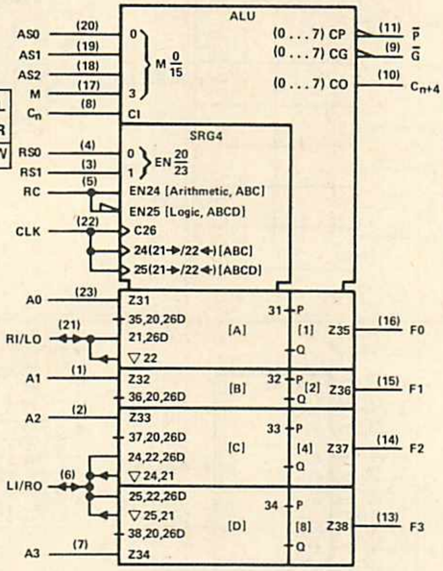
4-BIT PARALLEL BINARY ACCUMULATORS

typical performance

TYPE	ADD TIME	TOTAL POWER
'S281	20 ns	720 mW

SN54S281 (J,FH)
SN74S281 (J,N,FN)

logic symbol†



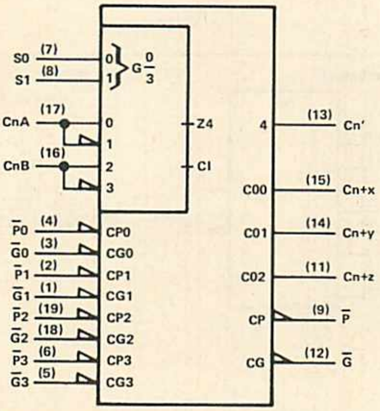
pin assignments

J,N PACKAGES				FH, FN PACKAGES			
1	A1	13	F3	1	nc	15	nc
2	A2	14	F2	2	A1	16	F3
3	RS1	15	F1	3	A2	17	F2
4	RS0	16	F0	4	RS1	18	F1
5	RC	17	M	5	RS0	19	F0
6	L1/R0	18	AS2	6	RC	20	M
7	A3	19	AS1	7	L1/R0	21	AS2
8	C_n	20	AS0	8	nc	22	nc
9	$\overline{G}$	21	R1/L0	9	A3	23	AS1
10	C_{n+4}	22	CLK	10	C_n	24	AS0
11	$\overline{P}$	23	A0	11	$\overline{G}$	25	R1/L0
12	GND	24	V_{CC}	12	C_{n+4}	26	CLK
				13	$\overline{P}$	27	A0
				14	GND	28	V_{CC}

282

LOOK-AHEAD CARRY GENERATOR WITH SELECTABLE CARRY INPUTS

logic symbol†



SN54AS282 (J,FH) SN74AS282 (N,FN)

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G1}$	11	C_{n+z}	1	$\overline{G1}$	11	C_{n+z}
2	$\overline{P1}$	12	G	2	$\overline{P1}$	12	G
3	$\overline{G0}$	13	$C_{n'}$	3	$\overline{G0}$	13	$C_{n'}$
4	$\overline{P0}$	14	C_{n+y}	4	$\overline{P0}$	14	C_{n+y}
5	$\overline{G3}$	15	C_{n+x}	5	$\overline{G3}$	15	C_{n+x}
6	$\overline{P3}$	16	CnB	6	$\overline{P3}$	16	CnB
7	S0	17	CnA	7	S0	17	CnA
8	S1	18	$\overline{G2}$	8	S1	18	$\overline{G2}$
9	$\overline{P}$	19	$\overline{P2}$	9	$\overline{P}$	19	$\overline{P2}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

283

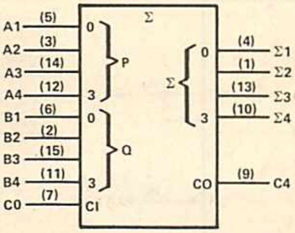
4-BIT BINARY FULL ADDERS

typical performance

TYPE	CARRY TIME	ADD TIME	POWER/ BIT
'283	10 ns	16 ns	76 mW
'LS283	10 ns	15 ns	24 mW
'S283	7 ns	11 ns	124 mW

SN54283 (J,FH) SN74283 (J,N)
SN54LS283 (J,FH) SN74LS283 (J,N,FN)
SN54S283 (J,FH) SN74S283 (J,N,FN)

logic symbol†



typical performance

J, N PACKAGES				FH, FN PACKAGES			
1	Σ2	9	C4	1	nc	11	nc
2	B2	10	Σ4	2	Σ2	12	C4
3	A2	11	B4	3	B2	13	Σ4
4	Σ1	12	A4	4	A2	14	B4
5	A1	13	Σ3	5	Σ1	15	A4
6	B1	14	A3	6	nc	16	nc
7	C0	15	B3	7	A1	17	Σ3
8	GND	16	V_{CC}	8	B1	18	A3
				9	C0	19	B3
				10	GND	20	V_{CC}

284

4-BIT BY 4-BIT PARALLEL BINARY MULTIPLIERS USED WITH '285

- MSB's for 4 X 4 multiplier ('285 provides LSB's)
- Use 'S274, 'LS275, 'S275 for new designs/larger multipliers

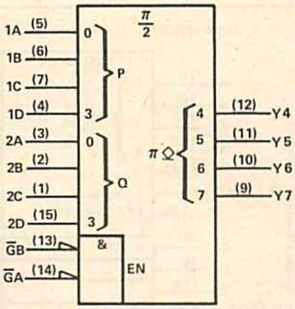
typical performance

TYPE	POWER	TIME*
'284	460 mW	40 ns

SN54284 (J,FH) SN74284 (J,N)

* 8-Bit Product Time

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	2C	9	Y7	1	nc	11	nc
2	2B	10	Y6	2	2C	12	Y7
3	2A	11	Y5	3	2B	13	Y6
4	1D	12	Y4	4	2A	14	Y5
5	1A	13	$\overline{GB}$	5	1D	15	Y4
6	1B	14	$\overline{GA}$	6	nc	16	nc
7	1C	15	2D	7	1A	17	$\overline{GB}$
8	GND	16	V_{CC}	8	1B	18	$\overline{GA}$
				9	1C	19	2D
				10	GND	20	V_{CC}

285

4-BIT BY 4-BIT PARALLEL BINARY MULTIPLIERS USED WITH '284

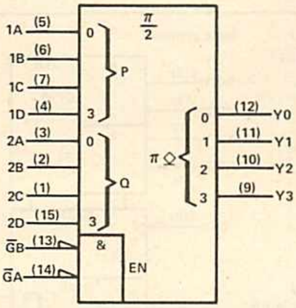
- LSB's for 4 X 4 multiplier ('284 provides MSB's)
- Use 'S274, 'LS275, 'S275 for new designs/larger multipliers

typical performance

TYPE	POWER
'285	460 mW

SN54285 (J,FH) SN74285 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	2C	9	Y3	1	nc	11	nc
2	2B	10	Y2	2	2C	12	Y3
3	2A	11	Y1	3	2B	13	Y2
4	1D	12	Y0	4	2A	14	Y1
5	1A	13	$\overline{GB}$	5	1D	15	Y0
6	1B	14	$\overline{GA}$	6	nc	16	nc
7	1C	15	2D	7	1A	17	$\overline{GB}$
8	GND	16	V_{CC}	8	1B	18	$\overline{GA}$
				9	1C	19	2D
				10	GND	20	V_{CC}

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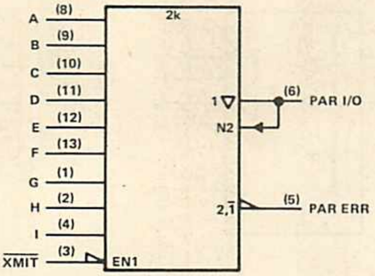
† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

286

9-BIT PARITY GENERATOR/CHECKER WITH BUS DRIVER PARITY I/O PORT

logic symbol†



SN54AS286 (J,FH)   SN74AS286 (N,FN)

pin assignments

J, N PACKAGE		FH, FN PACKAGE	
1 G	8 A	1 nc	11 nc
2 H	9 B	2 G	12 A
3 $\overline{\text{XMIT}}$	10 C	3 H	13 B
4 I	11 D	4 $\overline{\text{XMIT}}$	14 C
5 PARITY ERROR	12 E	5 nc	15 nc
6 PARITY I/O	13 F	6 I	16 D
7 GND	14 V_{CC}	7 nc	17 nc
		8 PARITY ERROR	18 E
		9 PARITY I/O	19 F
		10 GND	20 V_{CC}

For further information, contact the factory.

289

64-BIT RANDOM-ACCESS MEMORIES

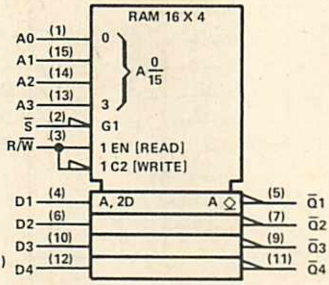
(16 4-bit words, open-collector outputs)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'LS289A	50 ns	35 ns	2.7 mW
'S289B	25 ns	12 ns	5.9 mW

SN54LS289A (J,FH)   SN74LS289A (J,N,FN)
SN54S289B (J,FH)   SN74S289B (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES		FH, FN PACKAGES	
1 A0	9 $\overline{\text{Q}}3$	1 nc	11 nc
2 $\overline{\text{S}}$	10 D3	2 A0	12 $\overline{\text{Q}}3$
3 R/$\overline{\text{W}}$	11 $\overline{\text{Q}}4$	3 $\overline{\text{S}}$	13 D3
4 D1	12 D4	4 R/$\overline{\text{W}}$	14 $\overline{\text{Q}}4$
5 $\overline{\text{Q}}1$	13 A3	5 D1	15 D4
6 D2	14 A2	6 nc	16 nc
7 $\overline{\text{Q}}2$	15 A1	7 $\overline{\text{Q}}1$	17 A3
8 GND	16 V_{CC}	8 D2	18 A2
		9 $\overline{\text{Q}}2$	19 A1
		10 GND	20 V_{CC}

290

DECADE COUNTERS

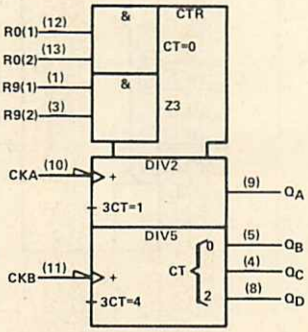
(divide-by-two and divide-by-five)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'290	32 MHz	HIGH	160 mW
'LS290	32 MHz	HIGH	40 mW

SN54290 (J,FH)   SN74290 (J,N)
SN54LS290 (J,FH)   SN74LS290 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES		FH, FN PACKAGES	
1 R9(1)	8 Q_D	1 nc	11 nc
2 nc	9 Q_A	2 R9(1)	12 Q_D
3 R9(2)	10 CKA	3 nc	13 Q_A
4 Q_C	11 CKB	4 R9(2)	14 CKA
5 Q_B	12 R0(1)	5 nc	15 nc
6 nc	13 R0(2)	6 Q_C	16 CKB
7 GND	14 V_{CC}	7 nc	17 nc
		8 Q_B	18 R0(1)
		9 nc	19 R0(2)
		10 GND	20 V_{CC}

292

PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

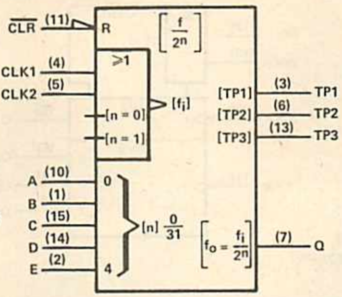
(digitally programmable from 2^2 to 2^{31})

typical performance

TYPE	POWER	f_{max}
'LS292	200 mW	50 MHz

SN54LS292 (J,FH) SN74LS292 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	B	9	nc
2	E	10	A
3	TP1	11	$\overline{\text{CLR}}$
4	CLK1	12	nc
5	CLK2	13	TP3
6	TP2	14	D
7	Q	15	C
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	B	12	nc
3	E	13	A
4	TP1	14	$\overline{\text{CLR}}$
5	CLK1	15	nc
6	nc	16	nc
7	CLK2	17	TP3
8	TP2	18	D
9	Q	19	C
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

293

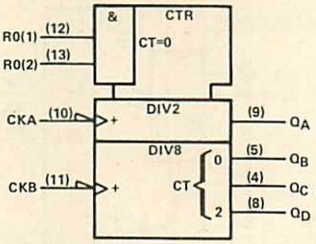
4-BIT BINARY COUNTERS
(divide-by-two and divide-by-eight)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'293	32 MHz	HIGH	160 mW
'LS293	32 MHz	HIGH	39 mW

SN54293 (J,FH) SN74293 (J,N)
SN54LS293 (J,FH) SN74LS293 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	nc	8	Q_D
2	nc	9	Q_A
3	nc	10	CKA
4	Q_C	11	CKB
5	Q_B	12	R0(1)
6	nc	13	R0(2)
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	nc	12	Q_D
3	nc	13	Q_A
4	nc	14	CKA
5	nc	15	nc
6	Q_C	16	CKB
7	nc	17	nc
8	Q_B	18	R0(1)
9	nc	19	R0(2)
10	GND	20	V_{CC}

294

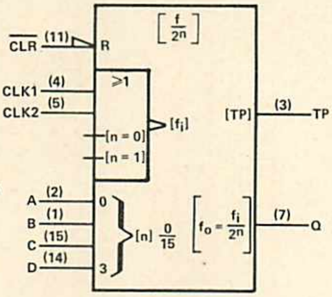
PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS
(digitally programmable from 2^2 to 2^{15})

typical performance

TYPE	POWER	f_{max}
'LS294	150 mW	50 MHz

SN54LS294 (J,FH) SN74LS294 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	B	9	nc
2	A	10	nc
3	TP	11	$\overline{CLR}$
4	CLK1	12	nc
5	CLK2	13	nc
6	nc	14	D
7	Q	15	C
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	B	12	nc
3	A	13	nc
4	TP	14	$\overline{CLR}$
5	CLK1	15	nc
6	nc	16	nc
7	CLK2	17	nc
8	nc	18	D
9	Q	19	C
10	GND	20	V_{CC}

295

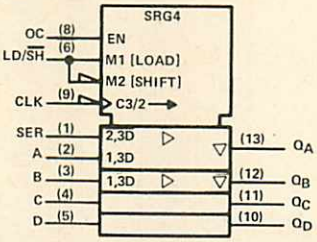
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	TOTAL POWER
'LS295B	30 MHz	D	70 mW

SN54LS295B (J,FH) SN74LS295B (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	SER	8	OC
2	A	9	CLK
3	B	10	Q_D
4	C	11	Q_C
5	D	12	Q_B
6	LD/$\overline{SH}$	13	Q_A
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	SER	12	OC
3	A	13	CLK
4	B	14	Q_D
5	nc	15	nc
6	C	16	Q_C
7	nc	17	nc
8	D	18	Q_B
9	LD/$\overline{SH}$	19	Q_A
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

297

DIGITAL PHASE-LOCKED-LOOP FILTERS

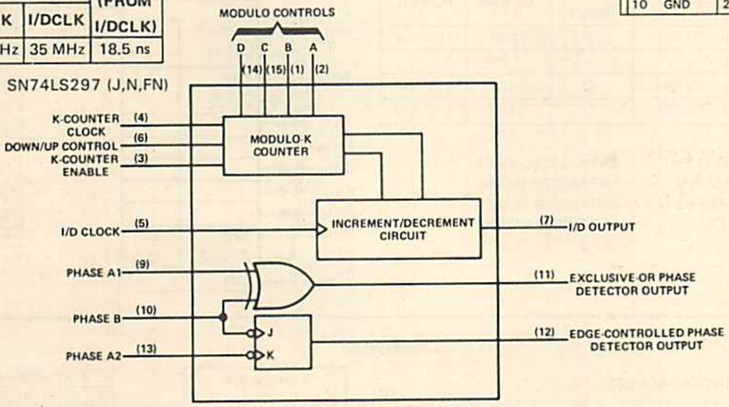
(cascadable for higher-order loops)

typical performance

TYPE	POWER	f_{max}		DELAY (FROM I/DCLK)
		KCLK	I/DCLK	
'LS297	375 mW	50 MHz	35 MHz	18.5 ns

SN54LS297 (J,FH) SN74LS297 (J,N,FN)

simplified block diagram†



pin assignments

J, N PACKAGES			
1	B	9	ϕA1
2	A	10	ϕB
3	ENCTR	11	XOPRD
4	K CLK	12	ECPD
5	I/D CLK	13	ϕA2
6	$D/\overline{U}$	14	D
7	I/D OUT	15	C
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	B	12	ϕA1
3	A	13	ϕB
4	ENCTR	14	XOPRD
5	K CLK	15	ECPD
6	nc	16	nc
7	I/D CLK	17	ϕA2
8	$D/\overline{U}$	18	D
9	I/D OUT	19	C
10	GND	20	V_{CC}

298

QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

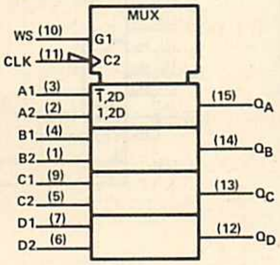
typical performance

TYPE	POWER	DELAY*
'298	195 mW	20 ns
'AS298		7.1 ns
'LS298	65 mW	20 ns

* From clock to non-inverted output

SN54298 (J,FH) SN74298 (J,N)
SN54AS298 (J,FH) SN74AS298 (N,FN)
SN54LS298 (J,FH) SN74LS298 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	B2	9	C1
2	A2	10	WS
3	A1	11	CLK
4	B1	12	Q_D
5	C2	13	Q_C
6	D2	14	Q_B
7	D1	15	Q_A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	B2	12	C1
3	A2	13	WS
4	A1	14	CLK
5	B1	15	Q_D
6	nc	16	nc
7	C2	17	Q_C
8	D2	18	Q_B
9	D1	19	Q_A
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

299

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTERS

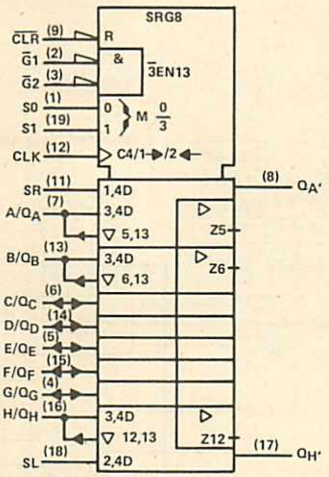
(three-state outputs)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'ALS299	30 MHz	D	LOW	100 mW
'AS299				
'LS299	35 MHz	D	LOW	175 mW
'S299	50 MHz	D	LOW	750 mW

SN54ALS299 (J,FH)	SN74ALS299 (N,FN)
SN54AS299 (J,FH)	SN74AS299 (N,FN)
SN54LS299 (J,FH)	SN74LS299 (J,N,FN)
SN54S299 (J,FH)	SN74S299 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	S0	11	SR
2	$\overline{G}1$	12	CLK
3	$\overline{G}2$	13	B/Q_B
4	G/Q_G	14	D/Q_D
5	E/Q_E	15	F/Q_F
6	C/Q_C	16	H/Q_H
7	A/Q_A	17	$Q_{H'}$
8	$Q_{A'}$	18	SL
9	$\overline{CLR}$	19	S1
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	S0	11	SR
2	$\overline{G}1$	12	CLK
3	$\overline{G}2$	13	B/Q_B
4	G/Q_G	14	D/Q_D
5	E/Q_E	15	F/Q_F
6	C/Q_C	16	H/Q_H
7	A/Q_A	17	$Q_{H'}$
8	$Q_{A'}$	18	SL
9	$\overline{CLR}$	19	S1
10	GND	20	V_{CC}

301

256-BIT RANDOM-ACCESS MEMORIES

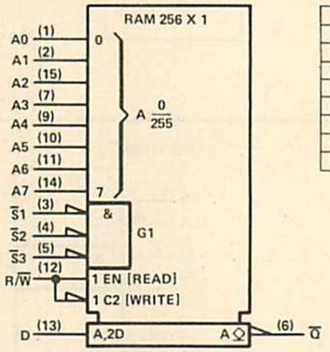
(256 1-bit words, open-collector output)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'S301	42 ns	13 ns	1.9 mW

SN74S301 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	9	A4
2	A1	10	A5
3	$\overline{S}1$	11	A6
4	$\overline{S}2$	12	R/$\overline{W}$
5	$\overline{S}3$	13	D
6	$\overline{Q}$	14	A7
7	A3	15	A2
8	GND	16	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

319

64-BIT RANDOM ACCESS MEMORIES

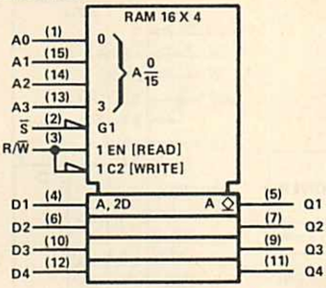
(16-four bit words, open-collector outputs)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER/ BIT
'LS319A	50 ns	35 ns	2.7 mW

SN54LS319A (J,FH) SN74LS319A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	9	Q3
2	$\overline{S}$	10	D3
3	R/$\overline{W}$	11	Q4
4	D1	12	D4
5	Q1	13	A3
6	D2	14	A2
7	Q2	15	A1
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	A0	12	Q3
3	$\overline{S}$	13	D3
4	R/$\overline{W}$	14	Q4
5	D1	15	D4
6	nc	16	nc
7	Q1	17	A3
8	D2	18	A2
9	Q2	19	A1
10	GND	20	V_{CC}

320

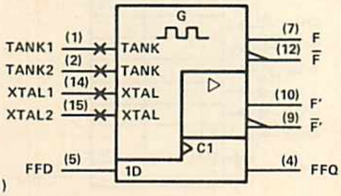
CRYSTAL-CONTROLLED OSCILLATORS

typical performance

TYPE	f_{max}	POWER
'LS320	30 MHz	210 mW

SN54LS320 (J) SN74LS320 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	TANK1	9	$\overline{F}$'
2	TANK2	10	F'
3	GND1	11	$V_{CC'}$
4	FFQ	12	$\overline{F}$
5	FFD	13	nc
6	nc	14	XTAL1
7	F	15	XTAL2
8	GND2	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	TANK1	12	$\overline{F}$'
3	TANK2	13	F'
4	GND1	14	$V_{CC'}$
5	FFQ	15	$\overline{F}$
6	nc	16	nc
7	FFD	17	nc
8	nc	18	XTAL1
9	F	19	XTAL2
10	GND2	20	V_{CC}

321

CRYSTAL-CONTROLLED OSCILLATORS

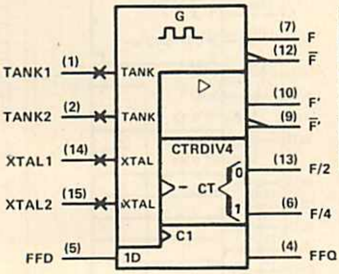
(with F/2 and F/4 count-down outputs)

typical performance

TYPE	FREQ	POWER
'LS321	30 MHz	235 mW

SN54LS321 (J) SN74LS321 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	TANK1	9	$\overline{F}$'
2	TANK2	10	F'
3	GND1	11	$V_{CC'}$
4	FFQ	12	$\overline{F}$
5	FFD	13	F/2
6	F/4	14	XTAL1
7	F	15	XTAL2
8	GND2	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	TANK1	12	$\overline{F}$'
3	TANK2	13	F'
4	GND1	14	$V_{CC'}$
5	FFQ	15	$\overline{F}$
6	nc	16	nc
7	FFD	17	F/2
8	F/4	18	XTAL1
9	F	19	XTAL2
10	GND2	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

322

8-BIT SHIFT REGISTERS WITH SIGN EXTEND

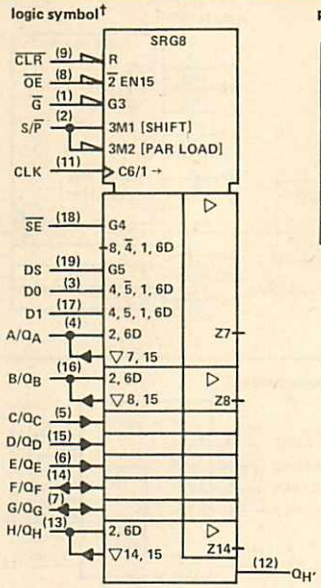
(three-state outputs, multiplexed I/O)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	POWER
'LS322A	35 MHz	D	LOW	175 mW

SN54LS322A (J,FH) SN74LS322A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$	11	CLK	1	$\overline{G}$	11	CLK
2	S/$\overline{P}$	12	$Q_{H'}$	2	S/$\overline{P}$	12	$Q_{H'}$
3	D0	13	H/Q_H	3	D0	13	H/Q_H
4	A/Q_A	14	F/Q_F	4	A/Q_A	14	F/Q_F
5	C/Q_C	15	D/Q_D	5	C/Q_C	15	D/Q_D
6	E/Q_E	16	B/Q_B	6	E/Q_E	16	B/Q_B
7	G/Q_G	17	D1	7	G/Q_G	17	D1
8	$\overline{OE}$	18	$\overline{SE}$	8	$\overline{OE}$	18	$\overline{SE}$
9	$\overline{CLR}$	19	DS	9	$\overline{CLR}$	19	DS
10	GND	20	V_{CC}	10	GND	20	V_{CC}

323

8-BIT BIDIRECTIONAL SHIFT/STORAGE REGISTERS

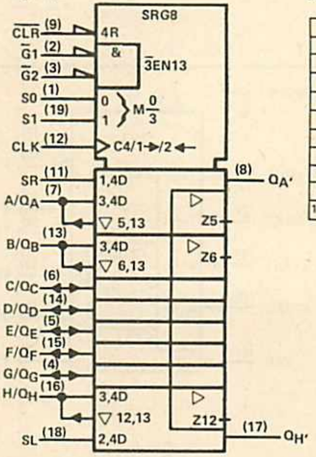
(three-state outputs)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	POWER
'ALS323	30 MHz	D	100 mW
'AS323			
'LS323	35 MHz	D	175 mW

SN54ALS323 (J,FH) SN74ALS323 (N,FN)
SN54AS323 (J,FH) SN74AS323 (N,FN)
SN54LS323 (J,FH) SN74LS323 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	S0	11	SR	1	S0	11	SR
2	$\overline{G}$1	12	CLK	2	$\overline{G}$1	12	CLK
3	$\overline{G}$2	13	B/Q_B	3	$\overline{G}$2	13	B/Q_B
4	G/Q_G	14	D/Q_D	4	G/Q_G	14	D/Q_D
5	E/Q_E	15	F/Q_F	5	E/Q_E	15	F/Q_F
6	C/Q_C	16	H/Q_H	6	C/Q_C	16	H/Q_H
7	A/Q_A	17	$Q_{H'}$	7	A/Q_A	17	$Q_{H'}$
8	$Q_{A'}$	18	SL	8	$Q_{A'}$	18	SL
9	$\overline{CLR}$	19	S1	9	$\overline{CLR}$	19	S1
10	GND	20	V_{CC}	10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

347

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

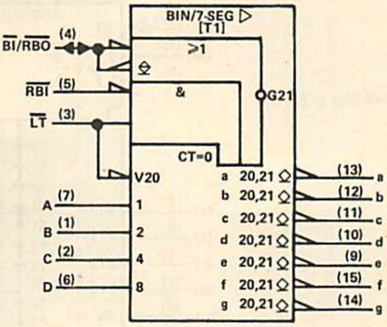
(open-collector outputs, low-voltage version of 'LS47)

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	POWER
SN54LS347	12 mA	7 V	35 mW
SN74LS347	24 mA	7 V	35 mW

SN54LS347 (J,FH) SN74LS347 (J,N, FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	B	9	e
2	C	10	d
3	$\overline{LT}$	11	c
4	$\overline{BI}/\overline{RBO}$	12	b
5	$\overline{RBI}$	13	a
6	D	14	g
7	A	15	f
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	B	12	e
3	C	13	d
4	$\overline{LT}$	14	c
5	$\overline{BI}/\overline{RBO}$	15	b
6	nc	16	nc
7	$\overline{RBI}$	17	a
8	D	18	g
9	A	19	f
10	GND	20	V_{CC}

348

8-LINE TO 3-LINE PRIORITY ENCODERS

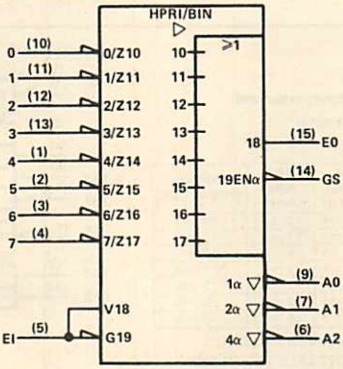
(with three-state outputs)

typical performance

TYPE	DELAY	POWER
'LS348	16 ns	63 mW

SN54LS348 (J,FH) SN74LS348 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	4	9	A0
2	5	10	0
3	6	11	1
4	7	12	2
5	E1	13	3
6	A2	14	GS
7	A1	15	E0
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	4	12	A0
3	5	13	0
4	6	14	1
5	7	15	2
6	nc	16	nc
7	E1	17	3
8	A2	18	GS
9	A1	19	E0
10	GND	20	V_{CC}

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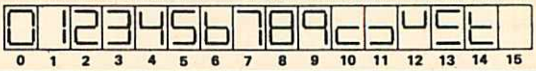
† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

FONT TABLE T1 – NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS USING 'LS347

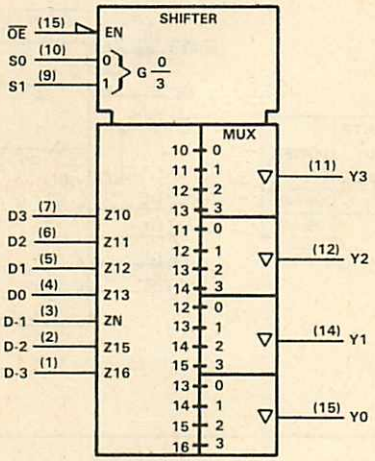


350

FOUR-BIT SHIFTER
(3-STATE OUTPUTS)

SN54S350 (J,FH) SN74S350 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	D-3	9	S1
2	D-2	10	S0
3	D-1	11	Y3
4	D0	12	Y2
5	D1	13	$\overline{OE}$
6	D2	14	Y1
7	D3	15	Y0
8	GND	16	V_{CC}

1	NC	11	NC
2	D-3	12	S1
3	D-2	13	S0
4	D-1	14	Y3
5	D0	15	Y2
6	NC	16	NC
7	D1	17	$\overline{OE}$
8	D2	18	Y1
9	D3	19	Y0
10	GND	20	V_{CC}

367

HEX BUS DRIVERS

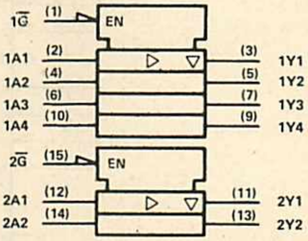
(non-inverted three-state outputs organized to facilitate handling of 4-bit data)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS367	7 ns	−12 mA	12 mA	53 mW
SN74ALS367	7 ns	−15 mA	24 mA	53 mW
SN74ALS367-1	7 ns	−15 mA	48 mA	53 mW
SN54367A	12 ns	−2 mA	32 mA	325 mW
SN74367A	12 ns	−5.2 mA	32 mA	325 mW
SN54LS367A	9.5 ns	−1 mA	12 mA	70 mW
SN74LS367A	9.5 ns	−2.6 mA	24 mA	70 mW

SN54367A (J,FH) SN74367A (J,N)
SN54ALS367 (J,FH) SN74ALS367 (N,FN)
SN74ALS367-1 (N,FN)
SN54LS367A (J,FH) SN74LS367A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$1\overline{G}$	9	1Y4
2	1A1	10	1A4
3	1Y1	11	2Y1
4	1A2	12	2A1
5	1Y2	13	2Y2
6	1A3	14	2A2
7	1Y3	15	$2\overline{G}$
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	$1\overline{G}$	12	1Y4
3	1A1	13	1A4
4	1Y1	14	2Y1
5	1A2	15	2A1
6	nc	16	nc
7	1Y2	17	2Y2
8	1A3	18	2A2
9	1Y3	19	$2\overline{G}$
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

NC — No internal connection.

351

DUAL 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

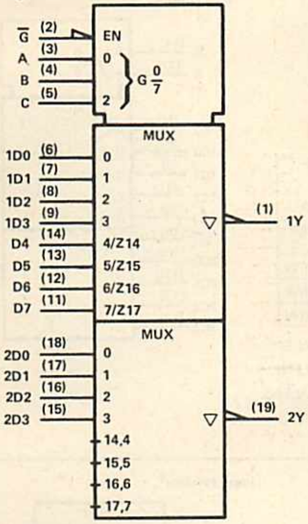
(three-state outputs; four common data inputs)

typical performance

TYPE	DELAY TIMES		TOTAL POWER
	DATA TO INV OUTPUT	FROM ENABLE	
'351	10 ns	17 ns	220 mW

SN74351 (J,N)

logic symbol†



pin assignments

J, N PACKAGES			
1	1Y	11	D7
2	$\overline{G}$	12	D6
3	A	13	D5
4	B	14	D4
5	C	15	2D3
6	1D0	16	2D2
7	1D1	17	2D1
8	1D2	18	2D0
9	1D3	19	2Y
10	GND	20	V_{CC}

352

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

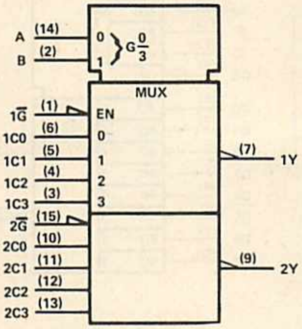
(inverting version of 'LS153)

typical performance

TYPE	DELAY TIMES		TOTAL POWER
	DATA TO INV OUTPUT	FROM ENABLE	
'ALS352	6 ns	4.5 ns	32.5 mW
'AS352	2.7 ns	4.5 ns	122.5 mW
'LS352	15 ns	18.5 ns	31 mW

SN54ALS352 (J,FH) SN74ALS352 (N,FN)
SN54AS352 (J,FH) SN74AS352 (N,FN)
SN54LS352 (J,FH) SN74LS352 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$1\overline{G}$	9	2Y
2	B	10	2C0
3	1C3	11	2C1
4	1C2	12	2C2
5	1C1	13	2C3
6	1C0	14	A
7	1Y	15	$2\overline{G}$
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	$1\overline{G}$	12	2Y
3	B	13	2C0
4	1C3	14	2C1
5	1C2	15	2C2
6	nc	16	nc
7	1C1	17	2C3
8	1C0	18	A
9	1Y	19	$2\overline{G}$
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

353

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

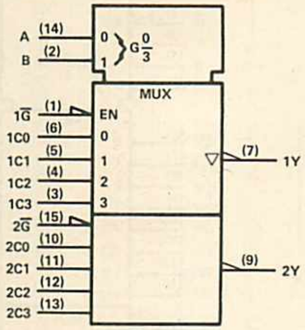
(three-state outputs, inverting version of 'LS253

typical performance

TYPE	DELAY TIMES		TOTAL POWER
	DATA TO INV OUTPUT	FROM ENABLE	
'ALS353	6 ns	4.5 ns	40 mW
'AS353	2.7 ns	5.5 ns	130 mW
'LS353	12 ns	13 ns	43 mW

SN54ALS353 (J,FH) SN74ALS353 (N,FN)
SN54AS353 (J,FH) SN74AS353 (N,FN)
SN54LS353 (J,FH) SN74LS353 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$1\overline{G}$	9	2Y	1	nc	11	nc
2	B	10	2C0	2	$1\overline{G}$	12	2Y
3	1C3	11	2C1	3	B	13	2C0
4	1C2	12	2C2	4	1C3	14	2C1
5	1C1	13	2C3	5	1C2	15	2C2
6	1C0	14	A	6	nc	16	nc
7	1Y	15	$2\overline{G}$	7	1C1	17	2C3
8	GND	16	V_{CC}	8	1C0	18	A
				9	1Y	19	$2\overline{G}$
				10	GND	20	V_{CC}

354

8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/ TRANSPARENT REGISTERS

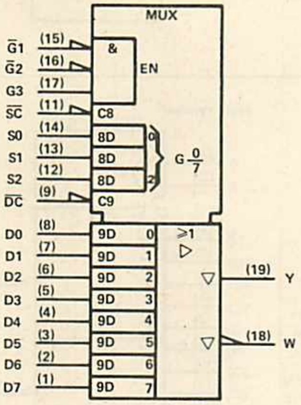
(three-state outputs)

typical performance

TYPE	DELAY TIMES		
	DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE
'LS354	23.5 ns	23.5 ns	16 ns

SN54LS354 (J,FH) SN74LS354 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D7	11	$\overline{SC}$	1	D7	11	$\overline{SC}$
2	D6	12	S2	2	D6	12	S2
3	D5	13	S1	3	D5	13	S1
4	D4	14	S0	4	D4	14	S0
5	D3	15	$\overline{G1}$	5	D3	15	$\overline{G1}$
6	D2	16	$\overline{G2}$	6	D2	16	$\overline{G2}$
7	D1	17	G3	7	D1	17	G3
8	D0	18	W	8	D0	18	W
9	$\overline{DC}$	19	Y	9	$\overline{DC}$	19	Y
10	GND	20	V_{CC}	10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

355

8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/ TRANSPARENT REGISTERS

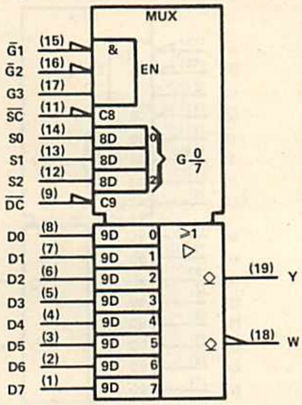
(open-collector outputs)

typical performance

DELAY TIMES		
DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE
31.5 ns	30 ns	21.5 ns

SN54LS355 (J,FH)   SN74LS355 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D7	11	$\overline{SC}$	1	D7	11	$\overline{SC}$
2	D6	12	S2	2	D6	12	S2
3	D5	13	S1	3	D5	13	S1
4	D4	14	S0	4	D4	14	S0
5	D3	15	$\overline{G}1$	5	D3	15	$\overline{G}1$
6	D2	16	$\overline{G}2$	6	D2	16	$\overline{G}2$
7	D1	17	G3	7	D1	17	G3
8	D0	18	W	8	D0	18	W
9	$\overline{DC}$	19	Y	9	$\overline{DC}$	19	Y
10	GND	20	V_{CC}	10	GND	20	V_{CC}

356

8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/ EDGE-TRIGGERED REGISTERS

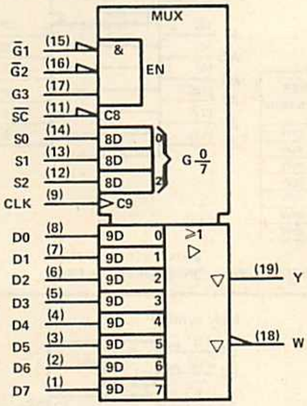
(three-state output)

typical performance

DELAY TIMES		
DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE
23.5 ns	23.5 ns	16 ns

SN54LS356 (J,FH)   SN74LS356 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D7	11	$\overline{SC}$	1	D7	11	$\overline{SC}$
2	D6	12	S2	2	D6	12	S2
3	D5	13	S1	3	D5	13	S1
4	D4	14	S0	4	D4	14	S0
5	D3	15	$\overline{G}1$	5	D3	15	$\overline{G}1$
6	D2	16	$\overline{G}2$	6	D2	16	$\overline{G}2$
7	D1	17	G3	7	D1	17	G3
8	D0	18	W	8	D0	18	W
9	CLK	19	Y	9	CLK	19	Y
10	GND	20	V_{CC}	10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

357

8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/ EDGE-TRIGGERED REGISTERS

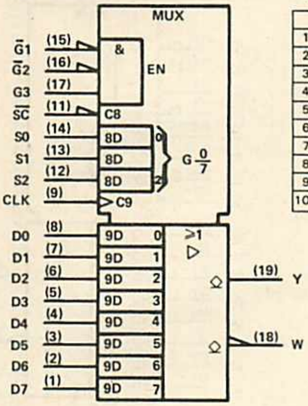
(open-collector outputs)

typical performance

DELAY TIMES		
DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE
31.5 ns	30 ns	25 ns

SN54LS357 (J,FH)   SN74LS357 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D7	11	$\overline{SC}$	1	D7	11	$\overline{SC}$
2	D6	12	S2	2	D6	12	S2
3	D5	13	S1	3	D5	13	S1
4	D4	14	S0	4	D4	14	S0
5	D3	15	$\overline{G}1$	5	D3	15	$\overline{G}1$
6	D2	16	$\overline{G}2$	6	D2	16	$\overline{G}2$
7	D1	17	G3	7	D1	17	G3
8	D0	18	W	8	D0	18	W
9	CLK	19	Y	9	CLK	19	Y
10	GND	20	V_{CC}	10	GND	20	V_{CC}

365

HEX BUS DRIVERS

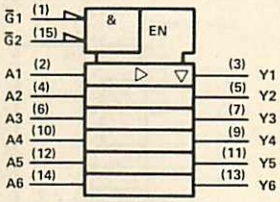
(non-inverted three-state outputs, gated enable inputs)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54365A	12 ns	−2 mA	32 mA	325 mW
SN74365A	12 ns	−5.2 mA	32 mA	325 mW
SN54ALS365	7 ns	−12 mA	12 mA	53 mW
SN74ALS365	7 ns	−15 mA	24 mA	53 mW
SN74ALS365-1	7 ns	−15 mA	48 mA	53 mW
SN54LS365A	9.5 ns	−1 mA	12 mA	70 mW
SN74LS365A	9.5 ns	−2.6 mA	24 mA	70 mW

SN54365A (J,FH)   SN74365A (J,N)   SN74ALS365-1 (N,FN)
SN54ALS365 (J,FH)   SN74ALS365 (N,FN)   SN54LS365A (J,FH)   SN74LS365A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}1$	9	Y4	1	nc	11	nc
2	A1	10	A4	2	$\overline{G}1$	12	Y4
3	Y1	11	Y5	3	A1	13	A4
4	A2	12	A5	4	Y1	14	Y5
5	Y2	13	Y6	5	A2	15	A5
6	A3	14	A6	6	nc	16	nc
7	Y3	15	$\overline{G}2$	7	Y2	17	Y6
8	GND	16	V_{CC}	8	A3	18	A6
				9	Y3	19	$\overline{G}2$
				10	GND	20	V_{CC}

366

HEX BUS DRIVERS

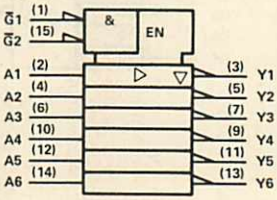
(inverted three-state outputs, gated enable inputs)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS366	5.5 ns	−12 mA	12 mA	40 mW
SN74ALS366	5.5 ns	−15 mA	24 mA	40 mW
SN74ALS366-1	5.5 ns	−15 mA	48 mA	40 mW
SN54366A	11 ns	−2 mA	32 mA	295 mW
SN74366A	11 ns	−5.2 mA	32 mA	295 mW
SN54LS366A	9.5 ns	−1 mA	12 mA	60 mW
SN74LS366A	9.5 ns	−2.6 mA	24 mA	60 mW

SN54366A (J,FH)   SN74366A (J,N)   SN74ALS366-1 (N,FN)
SN54ALS366 (J,FC)   SN74ALS366 (N,FN)   SN54LS366A (J,FH)   SN74LS366A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}1$	9	Y4	1	nc	11	nc
2	A1	10	A4	2	$\overline{G}1$	12	Y4
3	Y1	11	Y5	3	A1	13	A4
4	A2	12	A5	4	Y1	14	Y5
5	Y2	13	Y6	5	A2	15	A5
6	A3	14	A6	6	nc	16	nc
7	Y3	15	$\overline{G}2$	7	Y2	17	Y6
8	GND	16	V_{CC}	8	A3	18	A6
				9	Y3	19	$\overline{G}2$
				10	GND	20	V_{CC}

---

†Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

368

HEX BUS DRIVERS

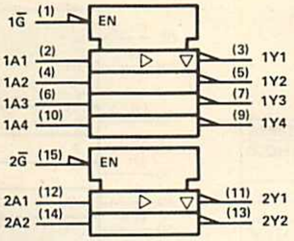
(inverted three-state outputs organized to facilitate handling of 4-bit data)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSIPATION
SN54ALS368	5.5 ns	−12 mA	12 mA	40 mW
SN74ALS368	5.5 ns	−15 mA	24 mA	40 mW
SN74ALS368-1	5.5 ns	−15 mA	48 mA	40 mW
SN54368A	11 ns	−2 mA	32 mA	295 mW
SN74368A	11 ns	−5.2 mA	32 mA	295 mW
SN54LS368A	9.5 ns	−1 mA	12 mA	60 mW
SN74LS368A	9.5 ns	−2.6 mA	24 mA	60 mW

SN54368A (J,FH)	SN74368A (J,N)
SN54ALS368 (J,FH)	SN74ALS368 (N,FN)
	SN74ALS368-1 (N,FN)
SN54LS368A (J,FH)	SN74LS368A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$1\overline{G}$	9	1Y4	1	nc	11	nc
2	1A1	10	1A4	2	$1\overline{G}$	12	1Y4
3	1Y1	11	2Y1	3	1A1	13	1A4
4	1A2	12	2A1	4	1Y1	14	2Y1
5	1Y2	13	2Y2	5	1A2	15	2A1
6	1A3	14	2A2	6	nc	16	nc
7	1Y3	15	$2\overline{G}$	7	1Y2	17	2Y2
8	GND	16	V_{CC}	8	1A3	18	2A2
				9	1Y3	19	$2\overline{G}$
				10	GND	20	V_{CC}

373

OCTAL D-TYPE LATCHES

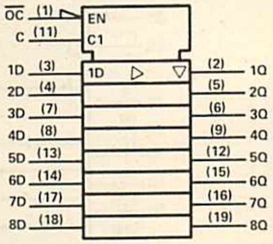
(three-state outputs, common output control, common enable)

typical performance

TYPE	OUT-PUTS	DELAY	TOTAL POWER
'ALS373	Q	8 ns	70 mW
'AS373			
'LS373	Q	19 ns	120 mW
'S373	Q	7 ns	525 mW

SN54ALS373 (J,FH)	SN74ALS373 (N,FN)
SN54AS373 (J,FH)	SN74AS373 (N,FN)
SN54LS373 (J,FH)	SN74LS373 (J,N,FN)
SN54S373 (J,FH)	SN74S373 (J,N,FN)

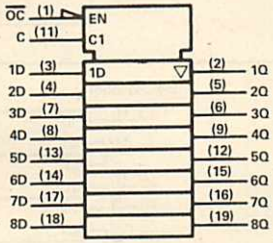
logic symbol, 'LS373, 'ALS373, 'AS373†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{OC}$	11	C	1	$\overline{OC}$	11	C
2	1Q	12	5Q	2	1Q	12	5Q
3	1D	13	5D	3	1D	13	5D
4	2D	14	6D	4	2D	14	6D
5	2Q	15	6Q	5	2Q	15	6Q
6	3Q	16	7Q	6	3Q	16	7Q
7	3D	17	7D	7	3D	17	7D
8	4D	18	8D	8	4D	18	8D
9	4Q	19	8Q	9	4Q	19	8Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol, 'S373†



† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

374

OCTAL D-TYPE FLIP-FLOPS

(three-state outputs, common output control, common clock)

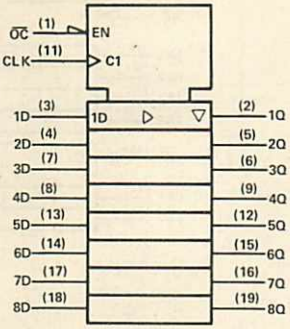
typical performance

TYPE	FREQ	POWER PER F-F	DATA TIMES	
			SET-UP	HOLD
'ALS374	50 MHz	10 mW		
'AS374				
'LS374	50 MHz	17 mW	20 ns†	0 ns†
'S374	100 MHz	56 mW	5 ns†	2 ns†

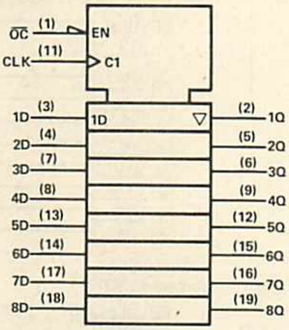
† Rising edge of clock pulse

SN54ALS374 (J,FH)	SN74ALS374 (N,FN)
SN54AS374 (J,FH)	SN74AS374 (N,FN)
SN54LS374 (J,FH)	SN74LS374 (J,N,FN)
SN54S374 (J,FH)	SN74S374 (J,N,FN)

logic symbol, 'LS374, 'ALS374, 'AS374



logic symbol, 'S374†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{OC}$	11	CLK	1	$\overline{OC}$	11	CLK
2	1Q	12	5Q	2	1Q	12	5Q
3	1D	13	5D	3	1D	13	5D
4	2D	14	6D	4	2D	14	6D
5	2Q	15	6Q	5	2Q	15	6Q
6	3Q	16	7Q	6	3Q	16	7Q
7	3D	17	7D	7	3D	17	7D
8	4D	18	8D	8	4D	18	8D
9	4Q	19	8Q	9	4Q	19	8Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

375

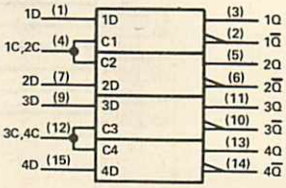
4-BIT BISTABLE LATCHES

typical performance

OUTPUTS	DELAY	TOTAL POWER
Q,$\overline{Q}$	12 ns	32 mW

SN54LS375 (J,FH)	SN74LS375 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1D	9	3D	1	nc	11	nc
2	$1\overline{Q}$	10	$3\overline{Q}$	2	1D	12	3D
3	1Q	11	3Q	3	$1\overline{Q}$	13	$3\overline{Q}$
4	1C,2C	12	3C,4C	4	1Q	14	3Q
5	2Q	13	4Q	5	1C,2C	15	3C,4C
6	$2\overline{Q}$	14	$4\overline{Q}$	6	nc	16	nc
7	2D	15	4D	7	2Q	17	4Q
8	GND	16	V_{CC}	8	$2\overline{Q}$	18	$4\overline{Q}$
				9	2D	19	4D
				10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

376

QUAD J-$\overline{K}$ FLIP-FLOPS

(common clock, common clear)

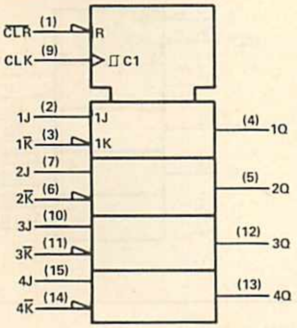
typical performance

FREQ	POWER PER F-F	DATA TIMES	
		SET-UP	HOLD
45 MHz	65 mW	0 ns†	20 ns†

† Rising edge of clock pulse

SN54376 (J,FH) SN74376 (J,N)

logic symbol†



pin assignments

J, N PACKAGES				FH PACKAGE			
1	$\overline{CLR}$	9	CLK	1	nc	11	nc
2	1J	10	3J	2	$\overline{CLR}$	12	CLK
3	1$\overline{K}$	11	3$\overline{K}$	3	1J	13	3J
4	1Q	12	3Q	4	1$\overline{K}$	14	3$\overline{K}$
5	2Q	13	4Q	5	1Q	15	3Q
6	2$\overline{K}$	14	4$\overline{K}$	6	nc	16	nc
7	2J	15	4J	7	2Q	17	4Q
8	GND	16	V_{CC}	8	2$\overline{K}$	18	4$\overline{K}$
				9	2J	19	4J
				10	GND	20	V_{CC}

377

OCTAL D-TYPE FLIP-FLOPS

(single-rail outputs, common enable, common clock)

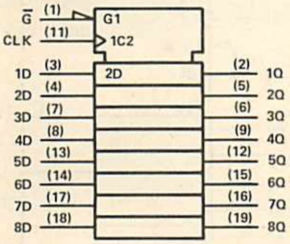
typical performance

FREQ	POWER PER F-F	DATA TIMES	
		SET-UP	HOLD
40 MHz	10.6 mW	20 ns†	5 ns†

† Rising edge of clock pulse

SN54LS377 (J,FH) SN74LS377 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$	11	CLK	1	$\overline{G}$	11	CLK
2	1Q	12	5Q	2	1Q	12	5Q
3	1D	13	5D	3	1D	13	5D
4	2D	14	6D	4	2D	14	6D
5	2Q	15	6Q	5	2Q	15	6Q
6	3Q	16	7Q	6	3Q	16	7Q
7	3D	17	7D	7	3D	17	7D
8	4D	18	8D	8	4D	18	8D
9	4Q	19	8Q	9	4Q	19	8Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

378

HEX D-TYPE FLIP-FLOPS

(single-rail outputs, common enable, common clock)

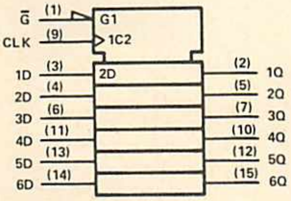
typical performance

FREQ	POWER PER F-F	DATA TIMES	
		SET-UP	HOLD
40 MHz	10.6 mW	20 ns†	5 ns†

† Rising edge of clock pulse

SN54LS378 (J,FH) SN74LS378 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$	9	CLK	1	nc	11	nc
2	1Q	10	4Q	2	$\overline{G}$	12	CLK
3	1D	11	4D	3	1Q	13	4Q
4	2D	12	5Q	4	1D	14	4D
5	2Q	13	5D	5	2D	15	5Q
6	3D	14	6D	6	nc	16	nc
7	3Q	15	6Q	7	2Q	17	5D
8	GND	16	V_{CC}	8	3D	18	6D
				9	3Q	19	6Q
				10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

379

QUAD D-TYPE FLIP-FLOPS

(double-rail outputs, common enable, common clock)

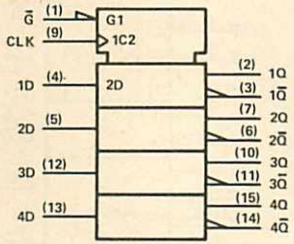
typical performance

FREQ	POWER PER F-F	DATA TIMES	
		SET-UP	HOLD
40 MHz	10.6 mW	20 ns†	5 ns†

† Rising edge of clock pulse

SN54LS379 (J,FH)
SN74LS379 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$	9	CLK	1	nc	11	nc
2	1Q	10	3Q	2	$\overline{G}$	12	CLK
3	$1\overline{Q}$	11	$3\overline{Q}$	3	1Q	13	3Q
4	1D	12	3D	4	$1\overline{Q}$	14	$3\overline{Q}$
5	2D	13	4D	5	1D	15	3D
6	$2\overline{Q}$	14	$4\overline{Q}$	6	nc	16	nc
7	2Q	15	4Q	7	2D	17	4D
8	GND	16	V_{CC}	8	$2\overline{Q}$	18	$4\overline{Q}$
				9	2Q	19	4Q
				10	GND	20	V_{CC}

381

ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS

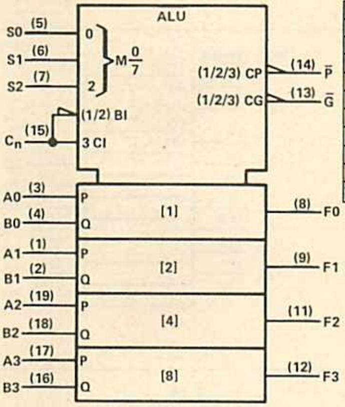
(8 binary functions, use 'S182 for look-ahead carry)

typical performance

TYPE	CARRY TIME	ADD TIME	TOTAL POWER
'LS381	16 ns	21 ns	175 mW
'S381	11 ns	20 ns	525 mW

SN54LS381 (J,FH)
SN54S381 (J,FH)
SN74LS381 (J,N,FN)
SN74S381 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A1	11	F2	1	A1	11	F2
2	B1	12	F3	2	B1	12	F3
3	A0	13	$\overline{G}$	3	A0	13	$\overline{G}$
4	B0	14	$\overline{P}$	4	B0	14	$\overline{P}$
5	S0	15	C_n	5	S0	15	C_n
6	S1	16	B3	6	S1	16	B3
7	S2	17	A3	7	S2	17	A3
8	F0	18	B2	8	F0	18	B2
9	F1	19	A2	9	F1	19	A2
10	GND	20	V_{CC}	10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

382

ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS

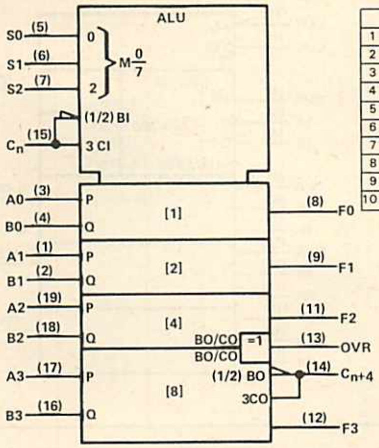
(ripple carry and overflow outputs)

typical performance

TYPE	CARRY TIME	ADD TIME	TOTAL POWER
'LS382	27 ns	18 ns	175 mW

SN54LS382 (J,FH)
SN74LS382 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	A1	11	F2	1	A1	11	F2
2	B1	12	F3	2	B1	12	F3
3	A0	13	OVR	3	A0	13	OVR
4	B0	14	C_{n+4}	4	B0	14	C_{n+4}
5	S0	15	C_n	5	S0	15	C_n
6	S1	16	B3	6	S1	16	B3
7	S2	17	A3	7	S2	17	A3
8	F0	18	B2	8	F0	18	B2
9	F1	19	A2	9	F1	19	A2
10	GND	20	V_{CC}	10	GND	20	V_{CC}

384

8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

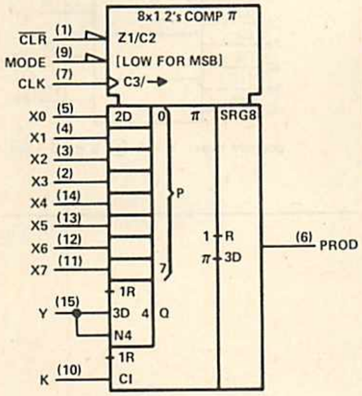
- Magnitude-only multiplication
- Cascadable for any number of bits
- Serial multiplier data input
- Serial data output for multiplication product
- 8-Bit parallel multiplicand data input
- 40 MHz typical max clock frequency

typical performance

MAX CLOCK FREQ	DELAY		TOTAL POWER
	FROM CLOCK	FROM CLEAR	
40 MHz	15 ns	17 ns	455 mW

SN54LS384 (J,FH)
SN74LS384 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{\text{CLR}}$	9	MODE	1	nc	11	nc
2	X3	10	K	2	$\overline{\text{CLR}}$	12	MODE
3	X2	11	X7	3	X3	13	K
4	X1	12	X6	4	X2	14	X7
5	X0	13	X5	5	X1	15	X6
6	PROD	14	X4	6	nc	16	nc
7	CLK	15	Y	7	X0	17	X5
8	GND	16	V_{CC}	8	PROD	18	X4
				9	CLK	19	Y
				10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

385

QUADRUPLE SERIAL ADDERS/ SUBTRACTORS

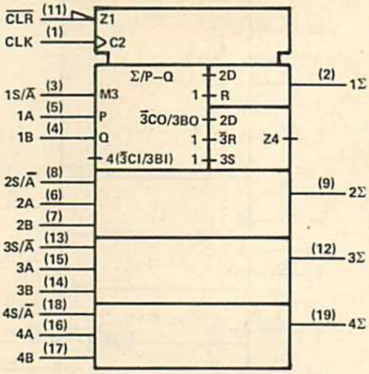
- Buffered clock, direct clear inputs
- Independent two's-complement addition/subtraction

typical performance

f_{max}	DELAY	POWER
40 MHz	16 ns	240 mW

SN54LS385 (J,FH)
SN74LS385 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	CLK	11	CLR	1	CLK	11	CLR
2	1Σ	12	3Σ	2	1Σ	12	3Σ
3	1S/$\overline{A}$	13	3S/$\overline{A}$	3	1S/$\overline{A}$	13	3S/$\overline{A}$
4	1B	14	3B	4	1B	14	3B
5	1A	15	3A	5	1A	15	3A
6	2A	16	4A	6	2A	16	4A
7	2B	17	4B	7	2B	17	4B
8	2S/$\overline{A}$	18	4S/$\overline{A}$	8	2S/$\overline{A}$	18	4S/$\overline{A}$
9	2Σ	19	4Σ	9	2Σ	19	4Σ
10	GND	20	V_{CC}	10	GND	20	V_{CC}

386

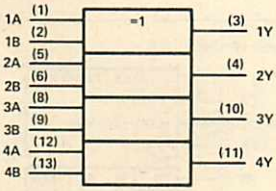
QUAD 2-INPUT EXCLUSIVE-OR GATES

typical performance

TYPE	DELAY	TOTAL POWER
'LS386	10 ns	30 mW

SN54LS386 (J,FH)
SN74LS386 (J,N,FN)

logic symbol†



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1A	8	3A	1	nc	11	nc
2	1B	9	3B	2	1A	12	3A
3	1Y	10	3Y	3	1B	13	3B
4	2Y	11	4Y	4	1Y	14	3Y
5	2A	12	4A	5	nc	15	nc
6	2B	13	4B	6	2Y	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4A
				9	2B	19	4B
				10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

390

DUAL DECADE COUNTERS

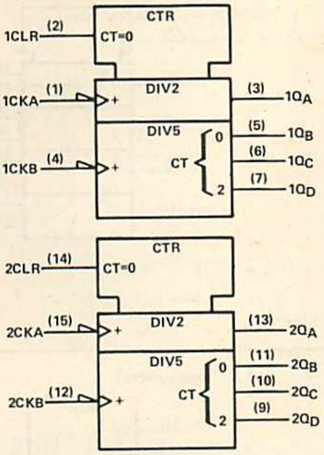
(bi-quinary or bcd sequences)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'390	25 MHz	HIGH	210 mW
'LS390	35 MHz	HIGH	75 mW

SN54390 (J,FH) SN74390 (J,N)
SN54LS390 (J,FH) SN74LS390 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1CKA	9	$2Q_D$
2	1CLR	10	$2Q_C$
3	$1Q_A$	11	$2Q_B$
4	1CKB	12	2CKB
5	$1Q_B$	13	$2Q_A$
6	$1Q_C$	14	2CLR
7	$1Q_D$	15	2CKA
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1CKA	12	$2Q_D$
3	1CLR	13	$2Q_C$
4	$1Q_A$	14	$2Q_B$
5	1CKB	15	2CKB
6	nc	16	nc
7	$1Q_B$	17	$2Q_A$
8	$1Q_C$	18	2CLR
9	$1Q_D$	19	2CKA
10	GND	20	V_{CC}

393

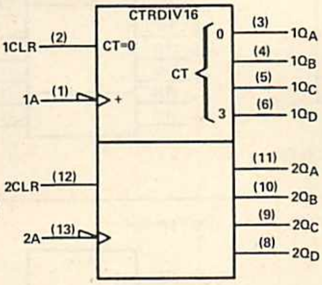
DUAL 4-BIT BINARY COUNTERS

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'393	25 MHz	HIGH	190 mW
'LS393	35 MHz	HIGH	75 mW

SN54393 (J,FH) SN74393 (J,N)
SN54LS393 (J,FH) SN74LS393 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1A	8	$2Q_D$
2	1CLR	9	$2Q_C$
3	$1Q_A$	10	$2Q_B$
4	$1Q_B$	11	$2Q_A$
5	$1Q_C$	12	2CLR
6	$1Q_D$	13	2A
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	$2Q_D$
3	1CLR	13	$2Q_C$
4	$1Q_A$	14	$2Q_B$
5	nc	15	nc
6	$1Q_B$	16	$2Q_A$
7	nc	17	nc
8	$1Q_C$	18	2CLR
9	$1Q_D$	19	2A
10	GND	20	V_{CC}

395

4-BIT UNIVERSAL SHIFT REGISTERS

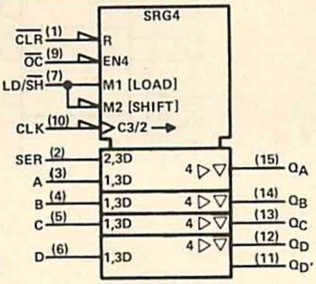
(three-state outputs)

typical performance

TYPE	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'AS395				
'LS395A	30 MHz	D	LOW	75 mW

SN54AS395 (J,FH) SN74AS395 (N,FN)
SN54LS395A (J,FH) SN74LS395A (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{CLR}$	9	$\overline{OC}$
2	SER	10	CLK
3	A	11	Q_D'
4	B	12	Q_D
5	C	13	Q_C
6	D	14	Q_B
7	LD/$\overline{SH}$	15	Q_A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	$\overline{CLR}$	12	$\overline{OC}$
3	SER	13	CLK
4	A	14	Q_D'
5	B	15	Q_D
6	nc	16	nc
7	C	17	Q_C
8	D	18	Q_B
9	LD/$\overline{SH}$	19	Q_A
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

396

OCTAL STORAGE REGISTERS

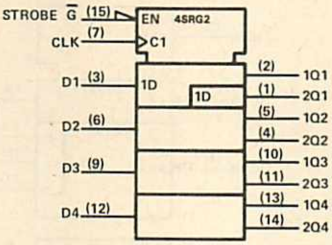
- Parallel access
- Applications:
  - N-bit storage files
  - HEX/BCD serial to parallel converters

typical performance

TYPE	MAX CLOCK FREQ	DELAY	POWER
'LS396	30 MHz	20 ns	120 mW

SN54LS396 (J,FH) SN74LS396 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	2Q1	9	D3	1	nc	11	nc
2	1Q1	10	1Q3	2	2Q1	12	D3
3	D1	11	2Q3	3	1Q1	13	1Q3
4	2Q2	12	D4	4	D1	14	2Q3
5	1Q2	13	1Q4	5	2Q2	15	D4
6	D2	14	2Q4	6	nc	16	nc
7	CLK	15	$\overline{G}$	7	1Q2	17	1Q4
8	GND	16	V_{CC}	8	D2	18	2Q4
				9	CLK	19	$\overline{G}$
				10	GND	20	V_{CC}

398

QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

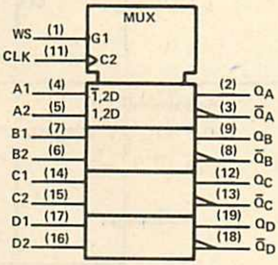
(double-rail outputs)

typical performance

TYPE	DELAY TIMES		TOTAL POWER
	CLOCK TO INV OUTPUT	CLOCK TO NON-INV OUTPUT	
'LS398	20 ns	20 ns	32 mW

SN54LS398 (J,FH) SN74LS398 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	WS	11	CLK	1	WS	11	CLK
2	Q_A	12	Q_C	2	Q_A	12	Q_C
3	$\overline{Q}_A$	13	$\overline{Q}_C$	3	$\overline{Q}_A$	13	$\overline{Q}_C$
4	A1	14	C1	4	A1	14	C1
5	A2	15	C2	5	A2	15	C2
6	B2	16	D2	6	B2	16	D2
7	B1	17	D1	7	B1	17	D1
8	$\overline{Q}_B$	18	$\overline{Q}_D$	8	$\overline{Q}_B$	18	$\overline{Q}_D$
9	Q_B	19	Q_D	9	Q_B	19	Q_D
10	GND	20	V_{CC}	10	GND	20	V_{CC}

399

QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

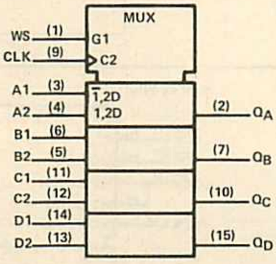
typical performance

TYPE	DELAY	TOTAL POWER
'LS399	20 ns*	37 mW

* From clock to output

SN54LS399 (J,FH) SN74LS399 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	WS	9	CLK	1	nc	11	nc
2	Q_A	10	Q_C	2	WS	12	CLK
3	A1	11	C1	3	Q_A	13	Q_C
4	A2	12	C2	4	A1	14	C1
5	B2	13	D2	5	A2	15	C2
6	B1	14	D1	6	nc	16	nc
7	Q_B	15	Q_D	7	B2	17	D2
8	GND	16	V_{CC}	8	B1	18	D1
				9	Q_B	19	Q_D
				10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

412

MULTI-MODE BUFFERED 8-BIT LATCHES

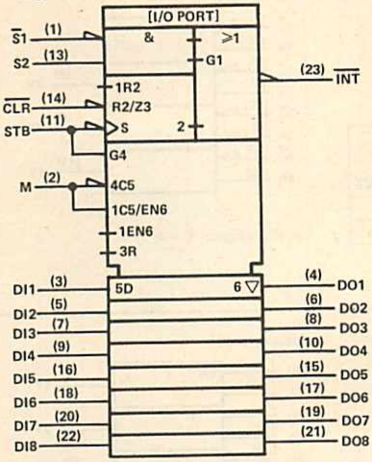
(three-state outputs; direct clear)

typical performance

CLEAR	OUT-PUTS	DELAY	TOTAL POWER
LOW	Q	11 ns	410 mW

SN54S412 (J,FH) SN74S412 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{\text{S1}}$	13	S2
2	M	14	$\overline{\text{CLR}}$
3	DI1	15	DO5
4	DO1	16	DI5
5	DI2	17	DO6
6	DO2	18	DI6
7	DI3	19	DO7
8	DO3	20	DI7
9	DI4	21	DO8
10	DO4	22	DI8
11	STB	23	$\overline{\text{INT}}$
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{\text{S1}}$	16	S2
3	M	17	$\overline{\text{CLR}}$
4	DI1	18	DO5
5	DO1	19	DI5
6	DI2	20	DO6
7	DO2	21	DI6
8	nc	22	nc
9	DI3	23	DO7
10	DO3	24	DI7
11	DI4	25	DO8
12	DO4	26	DI8
13	STB	27	$\overline{\text{INT}}$
14	GND	28	V_{CC}

422

RE-TRIGGERABLE MONO-STABLE MULTIVIBRATORS

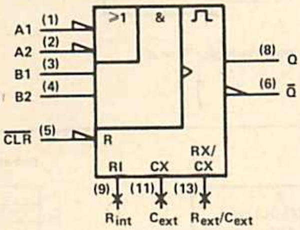
- Internal timing resistor
- Up to 100% duty cycle
- *Will not trigger from clear*

typical performance

NO. OF INPUTS		OUTPUT PULSE RANGE	TOTAL POWER
HIGH	LOW		
2	2	40 ns-∞	30 mW

SN54LS422 (J,FH) SN74LS422 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	A1	8	Q
2	A2	9	R_{int}
3	B1	10	nc
4	B2	11	C_{ext}
5	$\overline{\text{CLR}}$	12	nc
6	$\overline{\text{Q}}$	13	R_{ext}/C_{ext}
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	A1	12	Q
3	A2	13	R_{int}
4	B1	14	nc
5	nc	15	nc
6	B2	16	C_{ext}
7	nc	17	nc
8	$\overline{\text{CLR}}$	18	nc
9	$\overline{\text{Q}}$	19	R_{ext}/C_{ext}
10	GND	20	V_{CC}

423

RE-TRIGGERABLE MONO-STABLE MULTIVIBRATORS

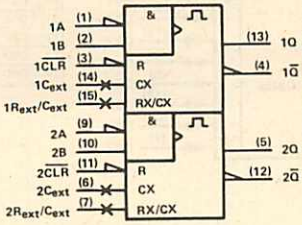
- Up to 100% duty cycle
- Will not trigger from clear

typical performance

NO. OF INPUTS		OUTPUT PULSE RANGE	TOTAL POWER
HIGH	LOW		
1	1	40 ns-∞	60 mW

SN54LS423 (J,FH) SN74LS423 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1A	9	2A
2	1B	10	2B
3	$1\overline{\text{CLR}}$	11	$2\overline{\text{CLR}}$
4	$1\overline{\text{Q}}$	12	$2\overline{\text{Q}}$
5	2Q	13	1Q
6	$2C_{ext}$	14	$1C_{ext}$
7	$2R_{ext}/C_{ext}$	15	$1R_{ext}/C_{ext}$
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	2A
3	1B	13	2B
4	$1\overline{\text{CLR}}$	14	$2\overline{\text{CLR}}$
5	$1\overline{\text{Q}}$	15	$2\overline{\text{Q}}$
6	nc	16	nc
7	2Q	17	1Q
8	$2C_{ext}$	18	$1C_{ext}$
9	$2R_{ext}/C_{ext}$	19	$1R_{ext}/C_{ext}$
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

425

QUAD GATES

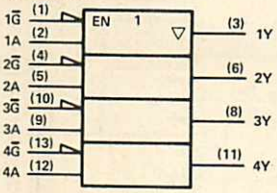
(three-state outputs, active-low enabling)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54425	10 ns	−2 mA	16 mA
SN74425	10 ns	−5.2 mA	16 mA

SN54425 (J,FH) SN74425 (J,N)

logic symbol†



positive logic: Y = A

pin assignments

J, N PACKAGES				FH PACKAGE			
1	$1\overline{G}$	8	3Y	1	nc	11	nc
2	1A	9	3A	2	$1\overline{G}$	12	3Y
3	1Y	10	$3\overline{G}$	3	1A	13	3A
4	$2\overline{G}$	11	4Y	4	1Y	14	$3\overline{G}$
5	2A	12	4A	5	nc	15	nc
6	2Y	13	$4\overline{G}$	6	$2\overline{G}$	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4A
				9	2Y	19	$4\overline{G}$
				10	GND	20	V_{CC}

426

QUAD GATES

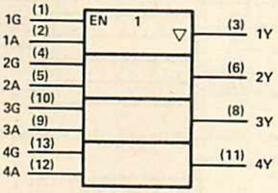
(three-state outputs, active-high enabling)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54426	10 ns	−2 mA	16 mA
SN74426	10 ns	−5.2 mA	16 mA

SN54426 (J,FH) SN74426 (J,N)

logic symbol†



positive logic: Y = A

pin assignments

J, N PACKAGES				FH PACKAGE			
1	1G	8	3Y	1	nc	11	nc
2	1A	9	3A	2	1G	12	3Y
3	1Y	10	3G	3	1A	13	3A
4	2G	11	4Y	4	1Y	14	3G
5	2A	12	4A	5	nc	15	nc
6	2Y	13	4G	6	2G	16	4Y
7	GND	14	V_{CC}	7	nc	17	nc
				8	2A	18	4A
				9	2Y	19	4G
				10	GND	20	V_{CC}

428

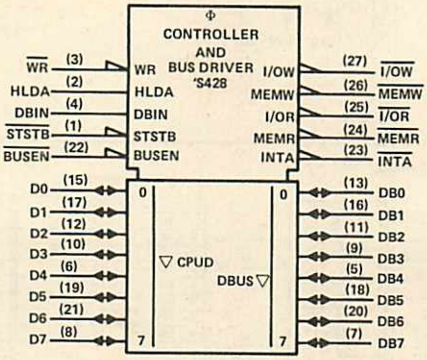
SYSTEM CONTROLLER FOR 8080A

typical performance

TYPE	POWER
'S428	700 mW

SN74S428 (J,N,FN)

logic symbol†



Φ
CONTROLLER AND BUS DRIVER 'S428
$\overline{WR}$ (3) WR
HLDA (2) HLDA
DBIN (4) DBIN
$\overline{STSTB}$ (1) STSTB
$\overline{BUSEN}$ (22) BUSEN
I/OW (27) $\overline{I/OW}$
MEMW (26) $\overline{MEMW}$
I/OR (25) $\overline{I/OR}$
MEMR (24) $\overline{MEMR}$
INTA (23) $\overline{INTA}$
D0 (15)
D1 (17)
D2 (12)
D3 (10)
D4 (6)
D5 (19)
D6 (21)
D7 (8)
0
7
▽ CPUD
DBUS ▽
0
7
(13) DB0
(16) DB1
(11) DB2
(9) DB3
(5) DB4
(18) DB5
(20) DB6
(7) DB7

pin assignments

J, N PACKAGES				FN PACKAGE			
1	$\overline{STSTB}$	15	D0	1	$\overline{STSTB}$	15	D0
2	HLDA	16	DB1	2	HLDA	16	DB1
3	$\overline{WR}$	17	D1	3	$\overline{WR}$	17	D1
4	DBIN	18	DB5	4	DBIN	18	DB5
5	DB4	19	D5	5	DB4	19	D5
6	D4	20	DB6	6	D4	20	DB6
7	DB7	21	D6	7	DB7	21	D6
8	D7	22	$\overline{BUSEN}$	8	D7	22	$\overline{BUSEN}$
9	DB3	23	$\overline{INTA}$	9	DB3	23	$\overline{INTA}$
10	D3	24	$\overline{MEMR}$	10	D3	24	$\overline{MEMR}$
11	DB2	25	$\overline{I/OR}$	11	DB2	25	$\overline{I/OR}$
12	D2	26	$\overline{MEMW}$	12	D2	26	$\overline{MEMW}$
13	DB0	27	$\overline{I/OW}$	13	DB0	27	$\overline{I/OW}$
14	GND	28	V_{CC}	14	GND	28	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

436, 437

LINE DRIVER/MEMORY DRIVER CIRCUITS – MOS MEMORY INTERFACE

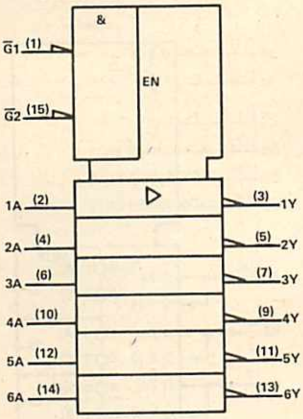
- Drives high-impedance loads
- Provides high-speed switching
- Requires minimum input current
- Damping output resistor for reducing transients ('436)
- Total power . . . 70 mW

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY
'S436	150 mA	−1 mA	5.5 ns
'S437	150 mA	−1 mA	5.5 ns

SN54S436 (J,FH) SN74S436 (J,N,FN)
SN54S437 (J,FH) SN74S437 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G1}$	9	4Y	1	nc	11	nc
2	1A	10	4A	2	$\overline{G1}$	12	4Y
3	1Y	11	5Y	3	1A	13	4A
4	2A	12	5A	4	1Y	14	5Y
5	2Y	13	6Y	5	2A	15	5A
6	3A	14	6A	6	nc	16	nc
7	3Y	15	$\overline{G2}$	7	2Y	17	6Y
8	GND	16	V_{CC}	8	3A	18	6A
				9	3Y	19	$\overline{G2}$
				10	GND	20	V_{CC}

QUAD TRIDIRECTIONAL BUS TRANSCEIVERS

440 (OPEN-COLLECTOR OUTPUTS, NONINVERTED LOGIC)
441 (OPEN-COLLECTOR OUTPUTS, INVERTED LOGIC)
442 (THREE-STATE OUTPUTS, NONINVERTED LOGIC)
443 (THREE-STATE OUTPUTS, INVERTED LOGIC)
444 (THREE-STATE OUTPUTS, INVERTED AND NONINVERTED LOGIC)

ALSO SEE 'LS448

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS440	22 ns	–	12 mA
SN74LS440	22 ns	–	24 mA
SN54LS441	15 ns	–	12 mA
SN74LS441	15 ns	–	24 mA
SN54LS442	11.5 ns	−12 mA	12 mA
SN74LS442	11.5 ns	−15 mA	24 mA
SN54LS443	8 ns	−12 mA	12 mA
SN74LS443	8 ns	−15 mA	24 mA
SN54LS444	9 ns	−12 mA	12 mA
SN74LS444	9 ns	−15 mA	24 mA

SN54LS440 (J,FH) SN74LS440 (J,FN)
SN54LS441 (J,FH) SN74LS441 (J,FN)
SN54LS442 (J,FH) SN74LS442 (J,FN)
SN54LS443 (J,FH) SN74LS443 (J,FN)
SN54LS444 (J,FH) SN74LS444 (J,FN)

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CS}$	11	S0	1	$\overline{CS}$	11	S0
2	B1	12	S1	2	B1	12	S1
3	C1	13	A4	3	C1	13	A4
4	C2	14	A3	4	C2	14	A3
5	B2	15	A2	5	B2	15	A2
6	B3	16	A1	6	B3	16	A1
7	C3	17	$\overline{GA}$	7	C3	17	$\overline{GA}$
8	C4	18	$\overline{GB}$	8	C4	18	$\overline{GB}$
9	B4	19	$\overline{GC}$	9	B4	19	$\overline{GC}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

For logic symbols see next two pages.

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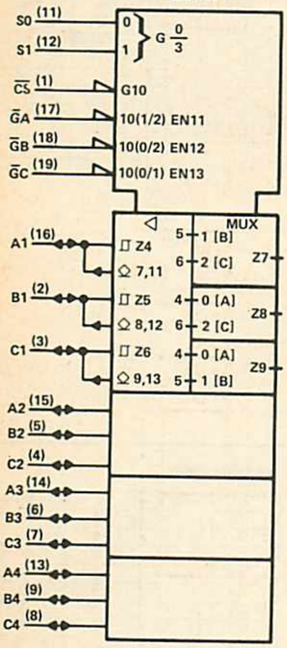
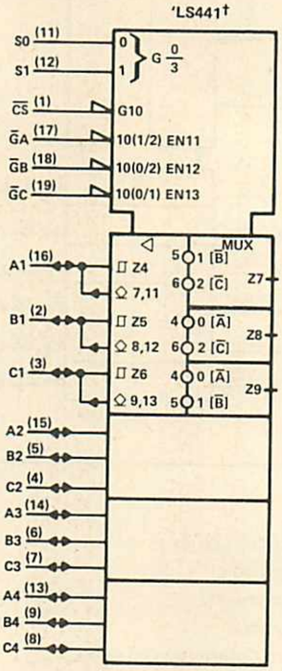
† Pin numbers shown on logic symbols are for J and N packages only.

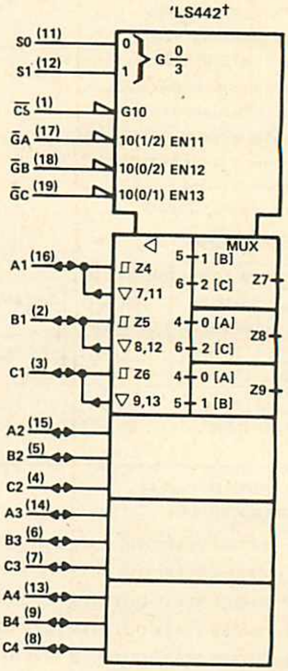
nc – no internal connection.

440, 441, 442, 443, 444 (continued)

logic symbol







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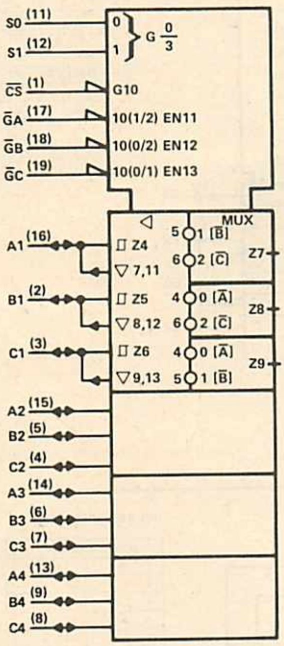
† Pin numbers shown on logic symbols are for J and N packages only.

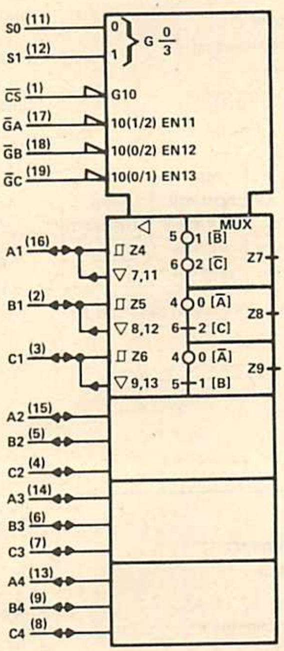
nc — no internal connection.

440, 441, 442, 443, 444 (continued)

'LS443†



'LS444†



445

BCD-TO-DECIMAL DECODERS/DRIVERS

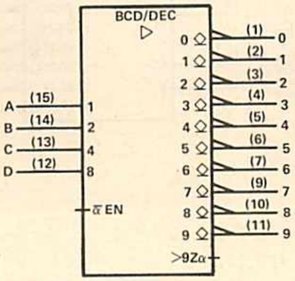
- Use as lamp, relay, or MOS driver
- Low-voltage version of 'LS145
- Full decoding of input logic
- All outputs off for invalid BCD input conditions

typical performance

OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
80 mA	7 V	35 mW

SN54LS445 (J,FH)   SN74LS445 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	0	9	7
2	1	10	8
3	2	11	9
4	3	12	D
5	4	13	C
6	5	14	B
7	6	15	A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	0	12	7
3	1	13	8
4	2	14	9
5	3	15	D
6	nc	16	nc
7	4	17	C
8	5	18	B
9	6	19	A
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

446

QUAD BUS TRANSCEIVERS WITH DIRECTION CONTROLS

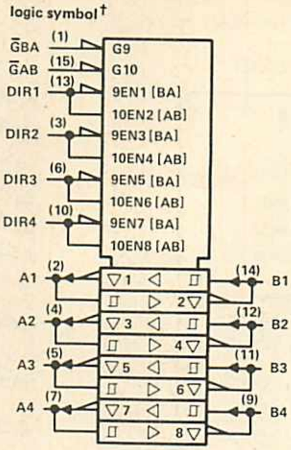
- Three-state outputs
- True ('LS449) and inverting ('LS446) outputs
- P-N-P inputs to reduce dc bus line loading

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS446	7.5 ns	−12 mA	12 mA
SN74LS446	7.5 ns	−15 mA	24 mA

SN54LS446 (J,FH) SN74LS446 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$BA	9	B4	1	nc	11	nc
2	A1	10	DIR4	2	$\overline{G}$BA	12	B4
3	DIR2	11	B3	3	A1	13	DIR4
4	A2	12	B2	4	DIR2	14	B3
5	A3	13	DIR1	5	A2	15	B2
6	DIR3	14	B1	6	nc	16	nc
7	A4	15	$\overline{G}$AB	7	A3	17	DIR1
8	GND	16	V_{CC}	8	DIR3	18	B1
				9	A4	19	$\overline{G}$AB
				10	GND	20	V_{CC}

447

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

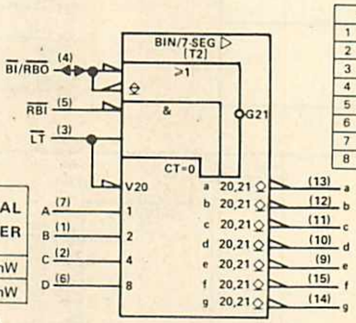
- Low-voltage version of 'LS247
- Open-collector outputs drive indicators directly
- Ripple blanking

typical performance

TYPE	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TOTAL POWER
SN54LS447	1.6 mA	7 V	35 mW
SN74LS447	3.2 mA	7 V	35 mW

SN54LS447 (J,FH) SN74LS447 (J,N,FN)

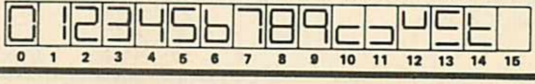
logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	B	9	e	1	nc	11	nc
2	C	10	d	2	B	12	e
3	$\overline{\text{LT}}$	11	c	3	C	13	d
4	$\overline{\text{BI}}/\overline{\text{RBO}}$	12	b	4	$\overline{\text{LT}}$	14	c
5	$\overline{\text{RBI}}$	13	a	5	$\overline{\text{BI}}/\overline{\text{RBO}}$	15	b
6	D	14	g	6	nc	16	nc
7	A	15	f	7	$\overline{\text{RBI}}$	17	a
8	GND	16	V_{CC}	8	D	18	g
				9	A	19	f
				10	GND	20	V_{CC}

FONT TABLE T2 – NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS USING '447



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† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

448

QUAD TRIDIRECTIONAL BUS TRANSCEIVERS

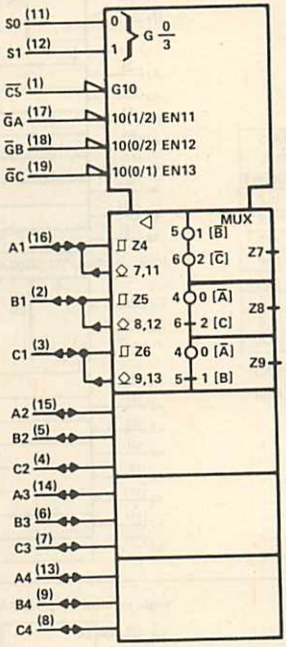
(OPEN-COLLECTOR OUTPUTS, INVERTED AND NONINVERTED LOGIC)

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS448	17.5 ns	–	12 mA
SN74LS448	17.5 ns	–	24 mA

SN54LS448 (J,FH) SN74LS448 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{\text{CS}}$	11	S0	1	$\overline{\text{CS}}$	11	S0
2	B1	12	S1	2	B1	12	S1
3	C1	13	A4	3	C1	13	A4
4	C2	14	A3	4	C2	14	A3
5	B2	15	A2	5	B2	15	A2
6	B3	16	A1	6	B3	16	A1
7	C3	17	$\overline{\text{GA}}$	7	C3	17	$\overline{\text{GA}}$
8	C4	18	$\overline{\text{GB}}$	8	C4	18	$\overline{\text{GB}}$
9	B4	19	$\overline{\text{GC}}$	9	B4	19	$\overline{\text{GC}}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

449

QUAD BUS TRANSCEIVERS WITH DIRECTION CONTROLS

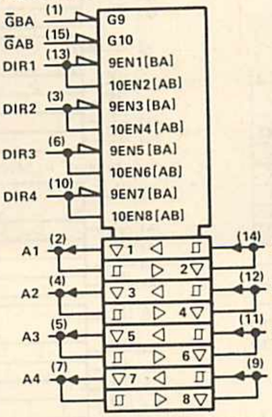
- Three-state outputs
- True ('LS449) and inverting ('LS446) outputs
- P-N-P inputs to reduce dc bus line loading

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54LS449	10.5 ns	−12 mA	12 mA
SN74LS449	10.5 ns	−15 mA	24 mA

SN54LS449 (J,FH) SN74LS449 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{\text{GBA}}$	9	B4
2	A1	10	DIR4
3	DIR2	11	B3
4	A2	12	B2
5	A3	13	DIR1
6	DIR3	14	B1
7	A4	15	$\overline{\text{GAB}}$
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	$\overline{\text{GBA}}$	12	B4
3	A1	13	DIR4
4	DIR2	14	B3
5	A2	15	B2
6	nc	16	nc
7	A3	17	DIR1
8	DIR3	18	B1
9	A4	19	$\overline{\text{GAB}}$
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

465, 466

OCTAL BUFFERS WITH THREE-STATE OUTPUTS

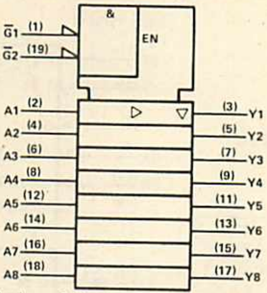
- P-N-P inputs reduce bus loading
- '465 true outputs
- '466 inverted outputs

typical performance

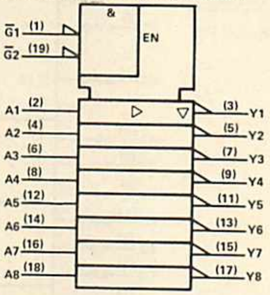
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS465A	7 ns	−12 mA	12 mA
SN74ALS465A	7 ns	−15 mA	24 mA
SN54ALS466A	7 ns	−12 mA	12 mA
SN74ALS466A	7 ns	−15 mA	24 mA
SN54LS465	11 ns	−1 mA	12 mA
SN74LS465	11 ns	−2.5 mA	24 mA
SN54LS466	8 ns	−1 mA	12 mA
SN74LS466	8 ns	−2.5 mA	24 mA

SN54ALS465A (J,FH)	SN74ALS465A (N,FN)
SN54ALS466A (J,FH)	SN74ALS466A (N,FN)
SN54LS465 (J)	SN74LS465 (J,N)
SN74LS466 (J)	SN74LS466 (J,N)

logic symbol, 'ALS465A, 'LS465†



logic symbol, 'ALS466A, 'LS466†



pin assignments

J, N PACKAGES			
1	$\overline{G1}$	11	Y5
2	A1	12	A5
3	Y1	13	Y6
4	A2	14	A6
5	Y2	15	Y7
6	A3	16	A7
7	Y3	17	Y8
8	A4	18	A8
9	Y4	19	$\overline{G2}$
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	$\overline{G1}$	11	Y5
2	A1	12	A5
3	Y1	13	Y6
4	A2	14	A6
5	Y2	15	Y7
6	A3	16	A7
7	Y3	17	Y8
8	A4	18	A8
9	Y4	19	$\overline{G2}$
10	GND	20	V_{CC}

467, 468

OCTAL BUFFERS WITH THREE-STATE OUTPUTS

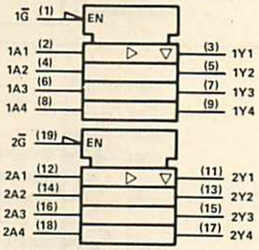
- P-N-P inputs reduce bus loading
- '467 true outputs
- '468 inverted outputs

typical performance

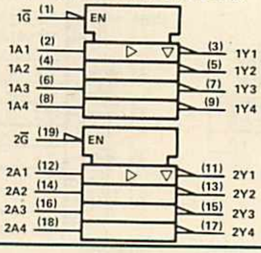
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS467A	7 ns	−12 mA	12 mA
SN74ALS467A	7 ns	−15 mA	24 mA
SN54ALS468A	7 ns	−12 mA	12 mA
SN74ALS468A	7 ns	−15 mA	24 mA
SN54LS467	11 ns	−1 mA	12 mA
SN74LS467	11 ns	−2.5 mA	24 mA
SN54LS468	8 ns	−1 mA	12 mA
SN74LS468	8 ns	−2.5 mA	24 mA

SN54ALS467A (J, FH)	SN74ALS467A (N,FN)
SN54ALS468A (J,FH)	SN74ASL468A (N,FN)
SN54LS467 (J)	SN74LS467 (J,N)
SN54LS468 (J)	SN74LS468 (J,N)

logic symbol, 'ALS467A, 'LS467 †



logic symbol, 'ALS468A, 'LS468



pin assignments

J, N PACKAGES			
1	$1\overline{G}$	11	2Y1
2	1A1	12	2A1
3	1Y1	13	2Y2
4	1A2	14	2A2
5	1Y2	15	2Y3
6	1A3	16	2A3
7	1Y3	17	2Y4
8	1A4	18	2A4
9	1Y4	19	$2\overline{G}$
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	$1\overline{G}$	11	2Y1
2	1A1	12	2A1
3	1Y1	13	2Y2
4	1A2	14	2A2
5	1Y2	15	2Y3
6	1A3	16	2A3
7	1Y3	17	2Y4
8	1A4	18	2A4
9	1Y4	19	$2\overline{G}$
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

481

4-BIT-SLICE CASCADABLE PROCESSOR ELEMENTS

typical performance

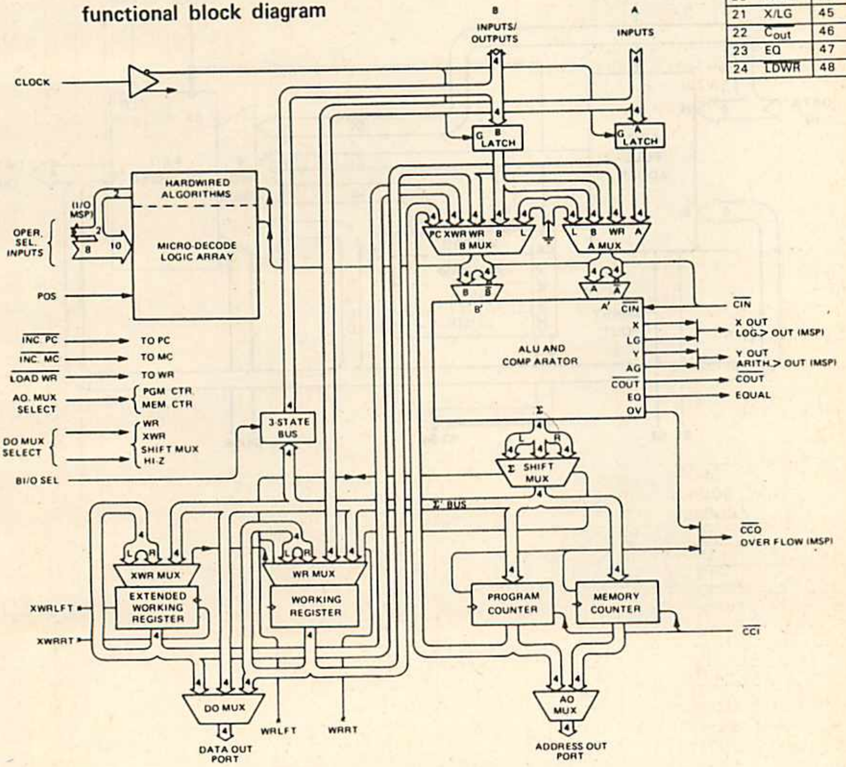
TYPE	OPERATION TIME
'LS481	120 ns
'S481	100 ns

SN74LS481 (J,N)
SN74S481 (J,N)

pin assignments

J, N PACKAGES			
1	B1/02	25	WRLFT
2	B1/03	26	WRRT
3	A13	27	XWRLFT
4	A12	28	XWRRT
5	A11	29	D0
6	A10	30	D1
7	OP0	31	DOP3
8	OP1	32	DOP2
9	OP2	33	DOP1
10	OP3	34	DOP0
11	OP7	35	$\overline{\text{INC MC}}$
12	V_{CC}	36	GND
13	OP6	37	$\overline{\text{CCO}}$/OV
14	OP5	38	AOP0
15	OP8	39	AOP1
16	PO9	40	AOP2
17	OP4	41	AOP3
18	$\overline{C_{in}}$	42	AOSEL
19	POS	43	$\overline{\text{INC PC}}$
20	Y/AG	44	$\overline{\text{CCI}}$
21	X/LG	45	CLK
22	$\overline{C_{out}}$	46	BI/O0
23	EQ	47	BI/O1
24	$\overline{\text{LDWR}}$	48	BI/O SEL

functional block diagram



482

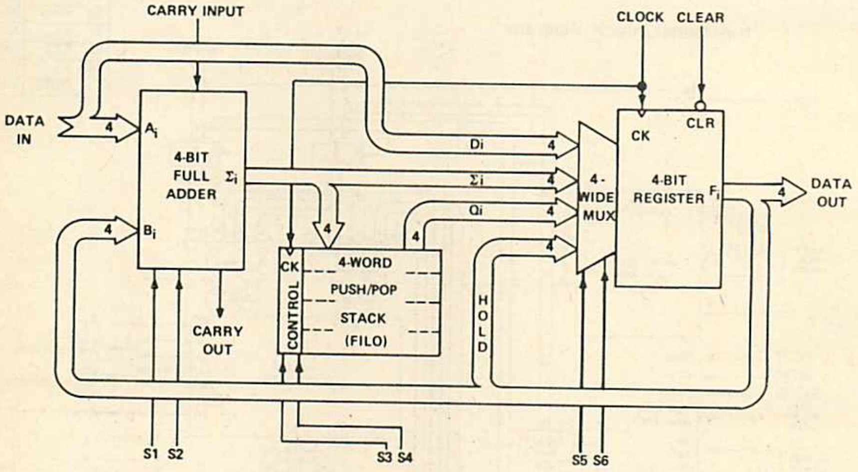
**4-BIT-SLICE
EXPANDABLE
CONTROL
ELEMENTS**

SN54S482 (J,FH)
SN74S482 (J,N,FN)

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	S4	11	A0	1	S4	11	A0
2	S3	12	F3	2	S3	12	F3
3	C_{out}	13	F2	3	C_{out}	13	F2
4	C_{in}	14	F1	4	C_{in}	14	F1
5	S1	15	F0	5	S1	15	F0
6	S2	16	$\overline{CLR}$	6	S2	16	$\overline{CLR}$
7	A3	17	S6	7	A3	17	S6
8	A2	18	S5	8	A2	18	S5
9	A1	19	CLK	9	A1	19	CLK
10	GND	20	V_{CC}	10	GND	20	V_{CC}

functional block diagram



nc — no internal connection.

484, 485

BCD-TO-BINARY AND BINARY-TO-BCD CODE CONVERTERS

('484 BCD-to-binary)
('485 binary-to-BCD)

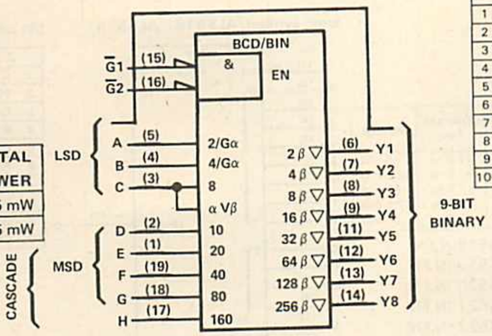
typical performance

TYPE	DELAY TIME PER PKG LEVEL	TOTAL POWER
'S484A	45 ns	525 mW
'S485A	45 ns	525 mW

SN54S484A (J,FH)
SN54S485A (J,N,FN)

SN74S484A (J,N,FN)
SN74S485A (J,N,FN)

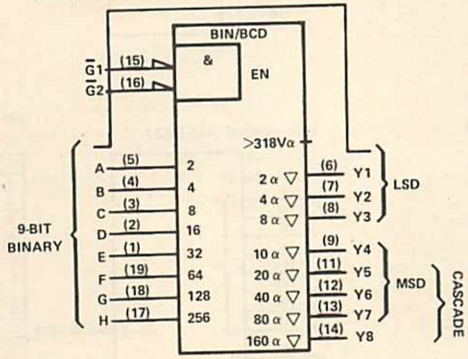
logic symbol 'S484A†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	E	11	Y5	1	E	11	Y5
2	D	12	Y6	2	D	12	Y6
3	C	13	Y7	3	C	13	Y7
4	B	14	Y8	4	B	14	Y8
5	A	15	$\overline{G1}$	5	A	15	$\overline{G1}$
6	Y1	16	$\overline{G2}$	6	Y1	16	$\overline{G2}$
7	Y2	17	H	7	Y2	17	H
8	Y3	18	G	8	Y3	18	G
9	Y4	19	F	9	Y4	19	F
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol 'S485A†



490

DUAL DECADE COUNTERS

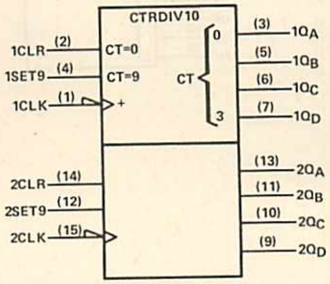
typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'490	25 MHz	HIGH	225 mW
'LS490	35 MHz	HIGH	75 mW

SN54490 (J,FH)
SN54LS490 (J,FH)

SN74490 (J,N)
SN74LS490 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	1CLK	9	$2Q_D$
2	1CLR	10	$2Q_C$
3	$1Q_A$	11	$2Q_B$
4	1SET9	12	2SET9
5	$1Q_B$	13	$2Q_A$
6	$1Q_C$	14	2CLR
7	$1Q_D$	15	2CLK
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1CLK	12	$2Q_D$
3	1CLR	13	$2Q_C$
4	$1Q_A$	14	$2Q_B$
5	1SET9	15	2SET9
6	nc	16	nc
7	$1Q_B$	17	$2Q_A$
8	$1Q_C$	18	2CLR
9	$1Q_D$	19	2CLK
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

518,519,520, 521,522

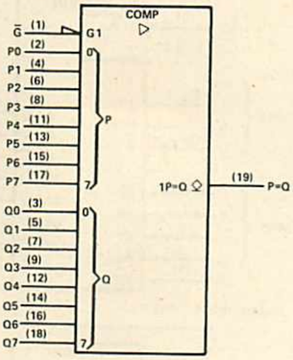
8-BIT IDENTITY COMPARATORS

- Compares two 8-bit words

TYPE	INPUT PULL-UP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION	COMPARE TIME	POWER
ALS518	yes	P = Q open-collector	17.5 ns	50 mW
ALS519	no	P = Q open-collector	17.5 ns	37.5 mW
ALS520	yes	$\overline{P=Q}$ totem-pole	9 ns	50 mW
ALS521	no	$\overline{P=Q}$ totem-pole	9 ns	37.5 mW
ALS522	yes	$\overline{P=Q}$ open-collector	15.5 ns	50 mW

SN54ALS518(J,FH)	SN74ALS518(N,FN)
SN54ALS519 (J,FH)	SN74ALS519 (N,FN)
SN54ALS520 (J,FH)	SN74ALS520 (N,FN)
SN54ALS521 (J,FH)	SN74ALS521 (N,FN)
SN54ALS522 (J,FH)	SN74ALS522 (N,FN)

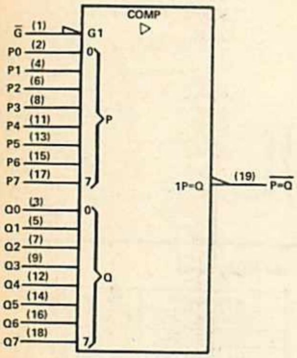
logic symbol 'ALS518, 'ALS519†



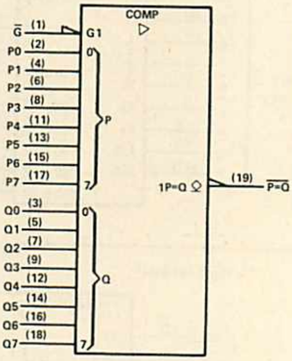
pin assignments, 'ALS518, 'ALS519

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$	11	P4	1	$\overline{G}$	11	P4
2	P0	12	Q4	2	P0	12	Q4
3	Q0	13	P5	3	Q0	13	P5
4	P1	14	Q5	4	P1	14	Q5
5	Q1	15	P6	5	Q1	15	P6
6	P2	16	Q6	6	P2	16	Q6
7	Q2	17	P7	7	Q2	17	P7
8	P3	18	Q7	8	P3	18	Q7
9	Q3	19	P = Q	9	Q3	19	P = Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol 'ALS520, 'ALS521†



logic symbol 'ALS522†



pin assignments, 'ALS520, 'ALS521, 'ALS522

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$	11	P4	1	$\overline{G}$	11	P4
2	P0	12	Q4	2	P0	12	Q4
3	Q0	13	P5	3	Q0	13	P5
4	P1	14	Q5	4	P1	14	Q5
5	Q1	15	P6	5	Q1	15	P6
6	P2	16	Q6	6	P2	16	Q6
7	Q2	17	P7	7	Q2	17	P7
8	P3	18	Q7	8	P3	18	Q7
9	Q3	19	$\overline{P=Q}$	9	Q3	19	$\overline{P=Q}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

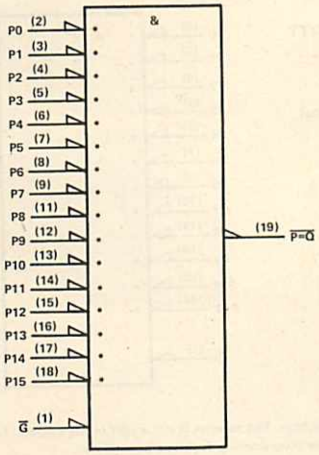
526

FUSE PROGRAMMABLE 16-BIT IDENTITY COMPARATOR

- Easy programmability
- Can be programmed and verified on most incoming test equipment
- High-speed address recognition

SN54ALS526 (J) SN74ALS526 (N)

logic diagram (positive logic)†



pin assignments

J,N PACKAGES			
1	$\overline{G}$	11	P8
2	P0	12	P9
3	P1	13	P10
4	P2	14	P11
5	P3	15	P12
6	P4	16	P13
7	P5	17	P14
8	P6	18	P15
9	P7	19	$\overline{P = Q}$
10	GND	20	V_{CC}

For chip carrier options and information, contact the factory.

* These inputs can be programmed to be active high. The asterisk is not a part of the symbol. For correct symbol for the programmed device, delete the polarity symbol (▷) at any input whose programming fuse has been blown.

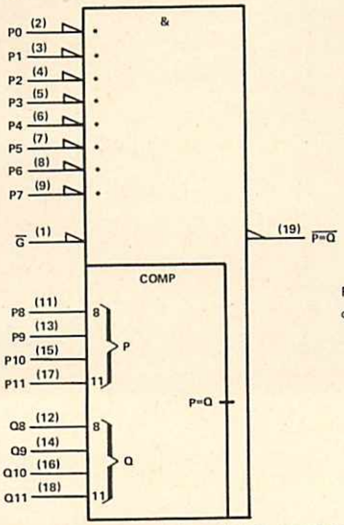
527

FUSE PROGRAMMABLE 8-BIT IDENTITY COMPARATOR AND 4-BIT COMPARATOR

- Easy programmability
- Can be programmed and verified on most incoming test equipment
- High-speed address recognition

SN54ALS527(J) SN74ALS527(N)

logic diagram (positive logic)†



pin assignments

J,N PACKAGES			
1	$\overline{G}$	11	P8
2	P0	12	Q8
3	P1	13	P9
4	P2	14	Q9
5	P3	15	P10
6	P4	16	Q10
7	P5	17	P11
8	P6	18	Q11
9	P7	19	$\overline{P = Q}$
10	GND	20	V_{CC}

For chip carrier options and information, contact the factory.

* These inputs can be programmed to be active high. The asterisk is not a part of the symbol. For correct symbol for the programmed device, delete the polarity symbol (▷) at any input whose programming fuse has been blown.

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

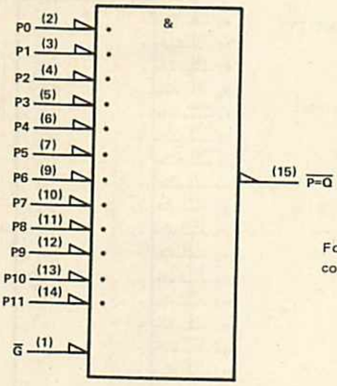
528

FUSE PROGRAMMABLE 12-BIT IDENTITY COMPARATOR

- Easy programmability
- Can be programmed and verified on most incoming test equipment
- High-speed address recognition

SN54ALS528(J) SN74ALS528 (N)

logic diagram (positive logic)†



pin assignments

J,N PACKAGES			
1	$\overline{G}$	9	P6
2	P0	10	P7
3	P1	11	P8
4	P2	12	P9
5	P3	13	P10
6	P4	14	P11
7	P5	15	$\overline{P=Q}$
8	GND	16	V_{CC}

For chip carrier options and information, contact the factory.

* These inputs can be programmed to be active high. The asterisk is not a part of the symbol. For correct symbol for the programmed device, delete the polarity symbol (▷) at any input whose programming fuse has been blown.

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†Pin numbers shown are for J and N packages.

533

OCTAL D-TYPE TRANSPARENT LATCHES

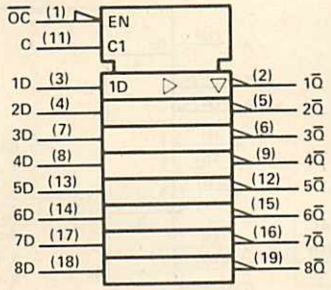
- Three-state buffer-type outputs drive bus lines directly
- Inverting outputs

typical performance

TYPE	OUT-PUTS	DELAY	TOTAL POWER
ALS533	$\overline{Q}$	10 ns	60 mW
AS533	$\overline{Q}$	5 ns	328 mW

SN54ALS533 (J,FH) SN74ALS533 (N,FN)
SN54AS533 (J,FH) SN74AS533 (N,FN)

logic symbol†



pin assignments

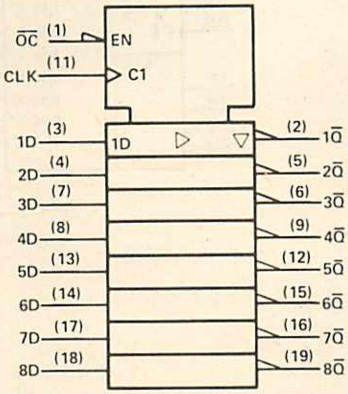
J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{OC}$	11	C	1	$\overline{OC}$	11	C
2	$\overline{1Q}$	12	$\overline{5Q}$	2	$\overline{1Q}$	12	$\overline{5Q}$
3	1D	13	5D	3	1D	13	5D
4	2D	14	6D	4	2D	14	6D
5	$\overline{2Q}$	15	$\overline{6Q}$	5	$\overline{2Q}$	15	$\overline{6Q}$
6	$\overline{3Q}$	16	$\overline{7Q}$	6	$\overline{3Q}$	16	$\overline{7Q}$
7	3D	17	7D	7	3D	17	7D
8	4D	18	8D	8	4D	18	8D
9	$\overline{4Q}$	19	$\overline{8Q}$	9	$\overline{4Q}$	19	$\overline{8Q}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

534

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- Three-state buffer-type outputs drive bus lines directly
- Inverting outputs

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{OC}$	11	CLK	1	$\overline{OC}$	11	CLK
2	$\overline{1Q}$	12	$\overline{5Q}$	2	$\overline{1Q}$	12	$\overline{5Q}$
3	1D	13	5D	3	1D	13	5D
4	2D	14	6D	4	2D	14	6D
5	$\overline{2Q}$	15	$\overline{6Q}$	5	$\overline{2Q}$	15	$\overline{6Q}$
6	$\overline{3Q}$	16	$\overline{7Q}$	6	$\overline{3Q}$	16	$\overline{7Q}$
7	3D	17	7D	7	3D	17	7D
8	4D	18	8D	8	4D	18	8D
9	$\overline{4Q}$	19	$\overline{8Q}$	9	$\overline{4Q}$	19	$\overline{8Q}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

typical performance

TYPE	F-MAX	PWR/ F/F	DATA TIMES	
			SET-UP	HOLD
'ALS534	50 MHz	10.4 mW	10 ns ↑	0 ns ↑
'AS534	165 MHz	51 mW	3 ns ↑	3 ns ↑

SN54ALS534 (J,FH) SN74ALS534 (N,FN)
SN54AS534 (J,FH) SN74AS534 (N,FN)

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†Pin numbers shown on logic symbols are for J and N packages only.

538

3- TO 8-LINE DECODERS/ DEMULTIPLEXERS

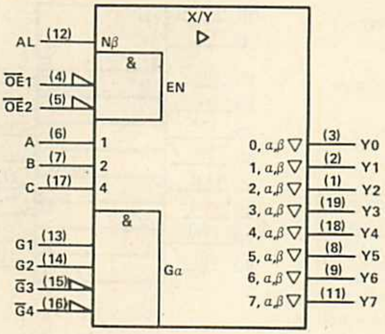
- Three-state outputs
- Output polarity control
- Multiple enables for expansion

typical performance

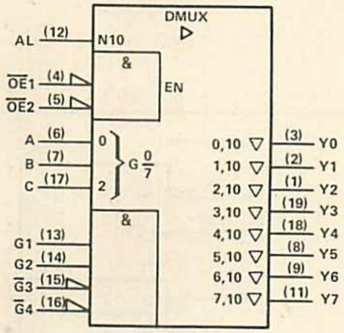
TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'ALS538			

SN54ALS538 (J,FH) SN74ALS538 (N, FN)

logic symbol†



OR



pin assignments

J, N PACKAGES			
1	Y2	11	Y7
2	Y1	12	AL
3	Y0	13	G1
4	$\overline{OE}$1	14	G2
5	$\overline{OE}$2	15	$\overline{G}$3
6	A	16	$\overline{G}$4
7	B	17	C
8	Y5	18	Y4
9	Y6	19	Y3
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	Y2	11	Y7
2	Y1	12	AL
3	Y0	13	G1
4	$\overline{OE}$1	14	G2
5	$\overline{OE}$2	15	$\overline{G}$3
6	A	16	$\overline{G}$4
7	B	17	C
8	Y5	18	Y4
9	Y6	19	Y3
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

539

2- TO 4-LINE DECODERS/ DEMULTIPLEXERS

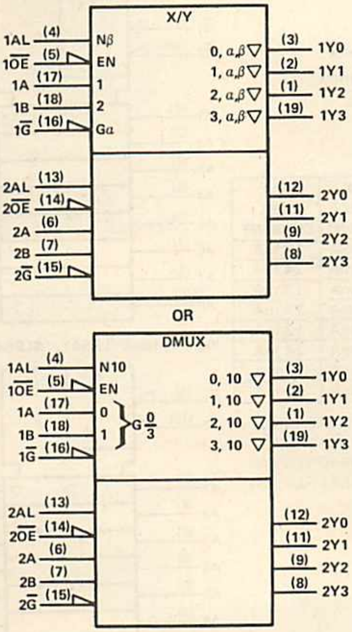
- Three-state outputs
- Output polarity control

typical performance

TYPE	SELECT TIME	ENABLE TIME	TOTAL POWER
'ALS539			

SN54ALS539 (J,FH)   SN74ALS539 (N, FN)

logic symbols†



pin assignments

J, N PACKAGES			
1	1Y2	11	2Y1
2	1Y1	12	2Y0
3	1Y0	13	2AL
4	1AL	14	2$\overline{\text{OE}}$
5	1$\overline{\text{OE}}$	15	2$\overline{\text{G}}$
6	2A	16	1$\overline{\text{G}}$
7	2B	17	1A
8	2Y3	18	1B
9	2Y2	19	1Y3
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1Y2	11	2Y1
2	1Y1	12	2Y0
3	1Y0	13	2AL
4	1AL	14	2$\overline{\text{OE}}$
5	1$\overline{\text{OE}}$	15	2$\overline{\text{G}}$
6	2A	16	1$\overline{\text{G}}$
7	2B	17	1A
8	2Y3	18	1B
9	2Y2	19	1Y3
10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

540, 541

OCTAL BUFFERS AND LINE DRIVERS

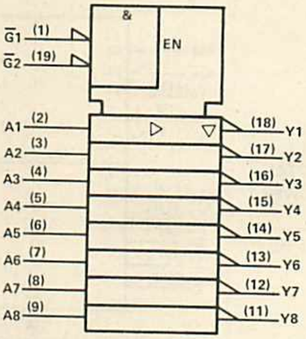
- Three-state output drives bus lines or buffer memory address registers
- 'LS540 for inverted data output
- 'LS541 for true data output

typical performance

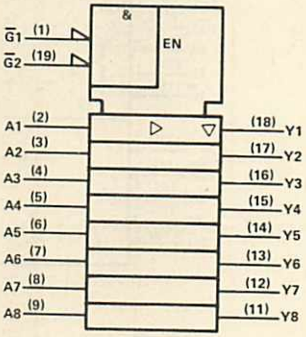
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS540	6 ns	−12 mA	12 mA
SN74ALS540	6 ns	−15 mA	24 mA
SN54ALS541	6 ns	−12 mA	12 mA
SN74ALS541	6 ns	−15 mA	24 mA
SN54LS540	9 ns	−12 mA	12 mA
SN74LS540	9.5 ns	−15 mA	24 mA
SN54LS541	9 ns	−12 mA	12 mA
SN74LS541	9.5 ns	−15 mA	24 mA

SN54ALS540 (J,FH)
SN54ALS541 (J,FH)
SN54LS540 (J,FH)
SN54LS541 ((J,FH)
SN74ALS540 (N,FN)
SN74ALS541 (N,FN)
SN74LS540 (J,N,FN)
SN74LS541 (J,N,FN)

logic symbol, 'LS540, 'ALS540†



logic symbol, 'LS541, 'ALS541†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}1$	11	Y8	1	$\overline{G}1$	11	Y8
2	A1	12	Y7	2	A1	12	Y7
3	A2	13	Y6	3	A2	13	Y6
4	A3	14	Y5	4	A3	14	Y5
5	A4	15	Y4	5	A4	15	Y4
6	A5	16	Y3	6	A5	16	Y3
7	A6	17	Y2	7	A6	17	Y2
8	A7	18	Y1	8	A7	18	Y1
9	A8	19	$\overline{G}2$	9	A8	19	$\overline{G}2$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

560

SYNCHRONOUS 4-BIT COUNTERS

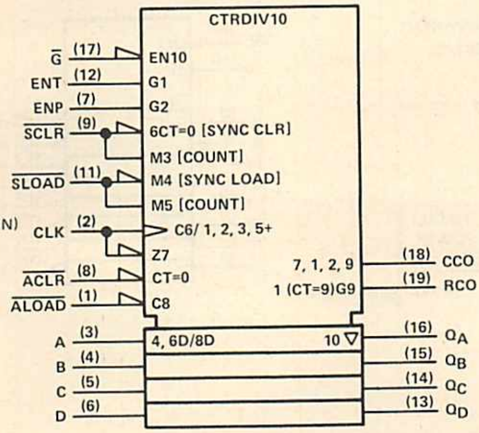
(decade, synchronous and asynchronous clear)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'ALS560A	30 MHz	Low	100 mW

SN54ALS560A (J,FH) SN74ALS560A (N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{\text{ALOAD}}$	11	$\overline{\text{SLOAD}}$
2	CLK	12	ENT
3	A	13	Q_D
4	B	14	Q_C
5	C	15	Q_B
6	D	16	Q_A
7	ENP	17	$\overline{\text{G}}$
8	$\overline{\text{ACLR}}$	18	CCO
9	$\overline{\text{SCLR}}$	19	RCO
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	$\overline{\text{ALOAD}}$	11	$\overline{\text{SLOAD}}$
2	CLK	12	ENT
3	A	13	Q_D
4	B	14	Q_C
5	C	15	Q_B
6	D	16	Q_A
7	ENP	17	$\overline{\text{G}}$
8	$\overline{\text{ACLR}}$	18	CCO
9	$\overline{\text{SCLR}}$	19	RCO
10	GND	20	V_{CC}

561

SYNCHRONOUS 4-BIT COUNTERS

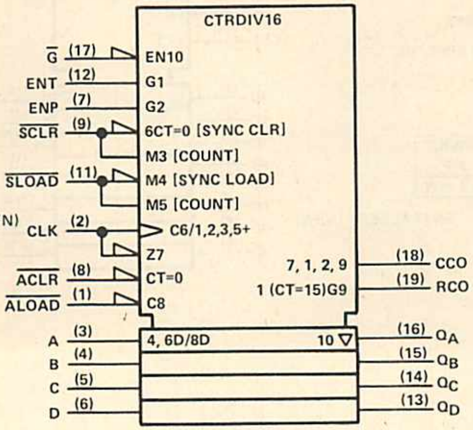
(binary, synchronous and asynchronous clear)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'ALS561A	40 MHz	Low	100 mW

SN54ALS561A (J,FH) AN74ALS561A (N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{\text{ALOAD}}$	11	$\overline{\text{SLOAD}}$
2	CLK	12	ENT
3	A	13	Q_D
4	B	14	Q_C
5	C	15	Q_B
6	D	16	Q_A
7	ENP	17	$\overline{\text{G}}$
8	$\overline{\text{ACLR}}$	18	CCO
9	$\overline{\text{SCLR}}$	19	RCO
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	$\overline{\text{ALOAD}}$	11	$\overline{\text{SLOAD}}$
2	CLK	12	ENT
3	A	13	Q_D
4	B	14	Q_C
5	C	15	Q_B
6	D	16	Q_A
7	ENP	17	$\overline{\text{G}}$
8	$\overline{\text{ACLR}}$	18	CCO
9	$\overline{\text{SCLR}}$	19	RCO
10	GND	20	V_{CC}

†Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

563

OCTAL D-TYPE TRANSPARENT LATCHES WITH INVERTED OUTPUTS

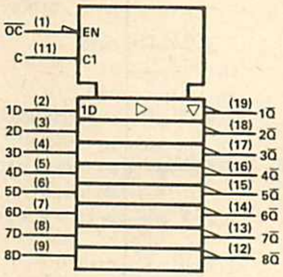
- Buffer-type outputs drive bus lines directly
- Inverted outputs

typical performance

TYPE	DELAY	TOTAL POWER
'ALS563	11 ns	67.5 mW

SN54ALS563 (J,FH) SN74ALS563 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{OC}$	11	C	1	$\overline{OC}$	11	C
2	1D	12	$8\overline{Q}$	2	1D	12	$8\overline{Q}$
3	2D	13	$7\overline{Q}$	3	2D	13	$7\overline{Q}$
4	3D	14	$6\overline{Q}$	4	3D	14	$6\overline{Q}$
5	4D	15	$5\overline{Q}$	5	4D	15	$5\overline{Q}$
6	5D	16	$4\overline{Q}$	6	5D	16	$4\overline{Q}$
7	6D	17	$3\overline{Q}$	7	6D	17	$3\overline{Q}$
8	7D	18	$2\overline{Q}$	8	7D	18	$2\overline{Q}$
9	8D	19	$1\overline{Q}$	9	8D	19	$1\overline{Q}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

564

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

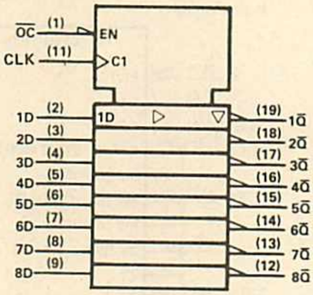
- Buffer-type outputs drive bus lines directly
- Inverted outputs

typical performance

TYPE	f_{max}	PWR/ F-F
'ALS564	50 MHz	8.4 mW

SN54ALS564 (J,FH) SN74ALS564 (N,FN)

logic symbol†



pin assignment

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{OC}$	11	CLK	1	$\overline{OC}$	11	CLK
2	1D	12	$8\overline{Q}$	2	1D	12	$8\overline{Q}$
3	2D	13	$7\overline{Q}$	3	2D	13	$7\overline{Q}$
4	3D	14	$6\overline{Q}$	4	3D	14	$6\overline{Q}$
5	4D	15	$5\overline{Q}$	5	4D	15	$5\overline{Q}$
6	5D	16	$4\overline{Q}$	6	5D	16	$4\overline{Q}$
7	6D	17	$3\overline{Q}$	7	6D	17	$3\overline{Q}$
8	7D	18	$2\overline{Q}$	8	7D	18	$2\overline{Q}$
9	8D	19	$1\overline{Q}$	9	8D	19	$1\overline{Q}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

†Pin numbers shown on logic symbols are for J and N packages only.

568

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

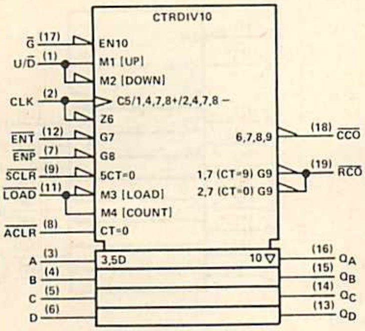
(decade, synchronous and asynchronous clear)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'ALS568A	30 MHz	Low	93 mW

SN54ALS568A (J,FH) SN74ALS568A (N,FN)

logic symbol†



pin assignment

J, N PACKAGES				FH, FN PACKAGES			
1	$U/\overline{D}$	11	$\overline{LOAD}$	1	$U/\overline{D}$	11	$\overline{LOAD}$
2	CLK	12	$\overline{ENT}$	2	CLK	12	$\overline{ENT}$
3	A	13	Q_D	3	A	13	Q_D
4	B	14	Q_C	4	B	14	Q_C
5	C	15	Q_B	5	C	15	Q_B
6	D	16	Q_A	6	D	16	Q_A
7	$\overline{ENP}$	17	$\overline{G}$	7	$\overline{ENP}$	17	$\overline{G}$
8	$\overline{ACLR}$	18	$\overline{CCO}$	8	$\overline{ACLR}$	18	$\overline{CCO}$
9	$\overline{SCLR}$	19	$\overline{RCO}$	9	$\overline{SCLR}$	19	$\overline{RCO}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

569

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

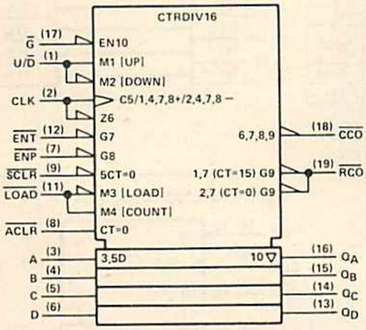
(binary, synchronous and asynchronous clear)

typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'ALS569A	40 MHz	Low	93 mW

SN54ALS569A (J,FH) SN74ALS569A (N,FN)

logic symbol†



pin assignment

J, N PACKAGES				FH, FN PACKAGES			
1	$U/\overline{D}$	11	$\overline{LOAD}$	1	$U/\overline{D}$	11	$\overline{LOAD}$
2	CLK	12	$\overline{ENT}$	2	CLK	12	$\overline{ENT}$
3	A	13	Q_D	3	A	13	Q_D
4	B	14	Q_C	4	B	14	Q_C
5	C	15	Q_B	5	C	15	Q_B
6	D	16	Q_A	6	D	16	Q_A
7	$\overline{ENP}$	17	$\overline{G}$	7	$\overline{ENP}$	17	$\overline{G}$
8	$\overline{ACLR}$	18	$\overline{CCO}$	8	$\overline{ACLR}$	18	$\overline{CCO}$
9	$\overline{SCLR}$	19	$\overline{RCO}$	9	$\overline{SCLR}$	19	$\overline{RCO}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

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†Pin numbers shown on logic symbols are for J and N packages only.

573

OCTAL D-TYPE TRANSPARENT LATCHES

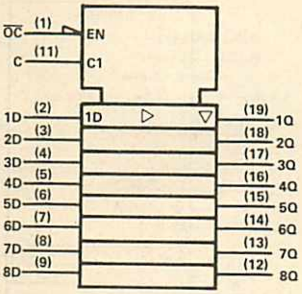
- Functionally equivalent to 'LS373 and 'S373
- Three-state buffer-type outputs drive bus lines directly
- Approximately half the power of 'LS373

typical performance

TYPE	OUT-PUTS	DELAY	TOTAL POWER
'ALS573	Q	11 ns	67.5 mW
'AS573	Q	4.5 ns	290 mW

SN54ALS573 (J,FH) SN74ALS573 (N,FN)
SN54AS573 (J,FH) SN74AS573 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{\text{OC}}$	11	C	1	$\overline{\text{OC}}$	11	C
2	1D	12	8Q	2	1D	12	8Q
3	2D	13	7Q	3	2D	13	7Q
4	3D	14	6Q	4	3D	14	6Q
5	4D	15	5Q	5	4D	15	5Q
6	5D	16	4Q	6	5D	16	4Q
7	6D	17	3Q	7	6D	17	3Q
8	7D	18	2Q	8	7D	18	2Q
9	8D	19	1Q	9	8D	19	1Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

574

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- Functionally equivalent to 'LS374 and 'S374
- Three-state buffer-type outputs drive bus lines directly
- Approximately half the power of 'LS374

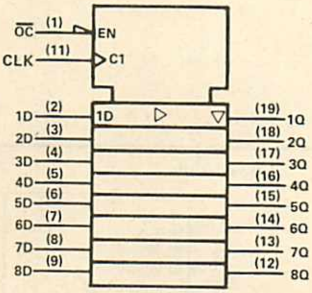
typical performance

TYPE	f_{max}	PWR/ F-F	DATA TIMES	
			SET-UP	HOLD
'ALS574	50 MHz	8.44 mW	10 ns†	4 ns†
'AS574	160 MHz	51 mW	3 ns†	3 ns†

† Rising edge of clock pulse

SN54ALS574 (J,FH) SN74ALS574 (N,FN)
SN54AS574 (J,FH) SN74AS574 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{\text{OC}}$	11	CLK	1	$\overline{\text{OC}}$	11	CLK
2	1D	12	8Q	2	1D	12	8Q
3	2D	13	7Q	3	2D	13	7Q
4	3D	14	6Q	4	3D	14	6Q
5	4D	15	5Q	5	4D	15	5Q
6	5D	16	4Q	6	5D	16	4Q
7	6D	17	3Q	7	6D	17	3Q
8	7D	18	2Q	8	7D	18	2Q
9	8D	19	1Q	9	8D	19	1Q
10	GND	20	V_{CC}	10	GND	20	V_{CC}

575

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- 3-state buffer-type outputs drive bus-lines directly
- Noninverting outputs

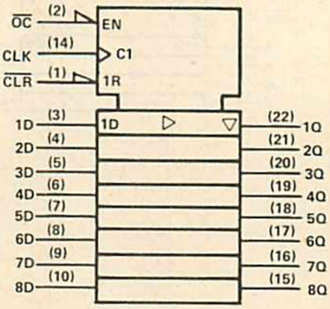
typical performance

TYPE	f_{max}	PWR/ F-F	DATA TIMES	
			SET-UP	HOLD
'ALS575	50 MHz	8.4 mW	10 ns†	4 ns†
'AS575	160 MHz	47 mW	3 ns†	3 ns†

† Rising edge of clock pulse

SN54ALS575 (J,FH) SN74ALS575 (N,FN)
SN54AS575 (J,FH) SN74AS575 (N,FN)

logic symbol, 'ALS575, 'AS575



pin assignment

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{\text{CLR}}$	13	nc	1	nc	15	nc
2	$\overline{\text{OC}}$	14	CLK	2	$\overline{\text{CLR}}$	16	nc
3	1D	15	8Q	3	$\overline{\text{OC}}$	17	CLK
4	2D	16	7Q	4	1D	18	8Q
5	3D	17	6Q	5	2D	19	7Q
6	4D	18	5Q	6	3D	20	6Q
7	5D	19	4Q	7	4D	21	5Q
8	6D	20	3Q	8	nc	22	nc
9	7D	21	2Q	9	5D	23	4Q
10	8D	22	1Q	10	6D	24	3Q
11	nc	23	nc	11	7D	25	2Q
12	GND	24	V_{CC}	12	8D	26	1Q
				13	nc	27	nc
				14	GND	28	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

576

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

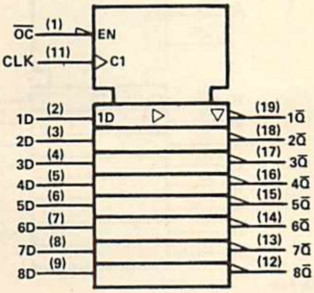
- Buffer-type outputs drive bus lines directly
- Inverted outputs

typical performance

TYPE	f_{max}	PWR/ F-F
'ALS576	50MHz	8.4 mW
'AS576	160MHz	

SN54ALS576 (J,FH) SN74ALS576 (N,FN)
SN54AS576 (J,FH) SN74AS576 (N,FN)

logic symbol†



pin assignments

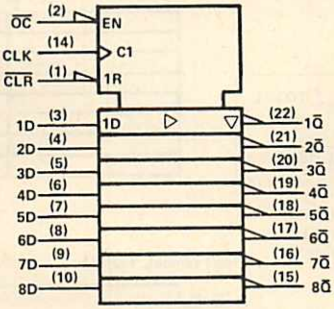
J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{OC}$	11	CLK	1	$\overline{OC}$	11	CLK
2	1D	12	$8\overline{Q}$	2	1D	12	$8\overline{Q}$
3	2D	13	$7\overline{Q}$	3	2D	13	$7\overline{Q}$
4	3D	14	$6\overline{Q}$	4	3D	14	$6\overline{Q}$
5	4D	15	$5\overline{Q}$	5	4D	15	$5\overline{Q}$
6	5D	16	$4\overline{Q}$	6	5D	16	$4\overline{Q}$
7	6D	17	$3\overline{Q}$	7	6D	17	$3\overline{Q}$
8	7D	18	$2\overline{Q}$	8	7D	18	$2\overline{Q}$
9	8D	19	$1\overline{Q}$	9	8D	19	$1\overline{Q}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

577

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- Buffer-type outputs drive bus lines directly
- Inverted outputs
- Synchronous clear

logic symbol, 'ALS577, 'AS577



pin assignment

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{CLR}$	13	nc	1	nc	15	nc
2	$\overline{OC}$	14	CLK	2	$\overline{CLR}$	16	nc
3	1D	15	$8\overline{Q}$	3	$\overline{OC}$	17	CLK
4	2D	16	$7\overline{Q}$	4	1D	18	$8\overline{Q}$
5	3D	17	$6\overline{Q}$	5	2D	19	$7\overline{Q}$
6	4D	18	$5\overline{Q}$	6	3D	20	$6\overline{Q}$
7	5D	19	$4\overline{Q}$	7	4D	21	$5\overline{Q}$
8	6D	20	$3\overline{Q}$	8	nc	22	nc
9	7D	21	$2\overline{Q}$	9	5D	23	$4\overline{Q}$
10	8D	22	$1\overline{Q}$	10	6D	24	$3\overline{Q}$
11	nc	23	nc	11	7D	25	$2\overline{Q}$
12	GND	24	V_{CC}	12	8D	26	$1\overline{Q}$
				13	nc	27	nc
				14	GND	28	V_{CC}

typical performance

TYPE	f_{max}	POWER/ F-F	DATA TIMES	
			SET-UP	HOLD
'ALS577	50 MHz	8.4 mW	10 ns†	4 ns†
'AS577	160 MHz			

†Rising edge of clock pulse

SN54ALS577 (J,FH) SN74ALS577(N,FN)
SN54AS577 (J,FH) SN74AS577(N,FN)

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†Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

580

OCTAL D-TYPE TRANSPARENT LATCHES WITH INVERTED OUTPUTS

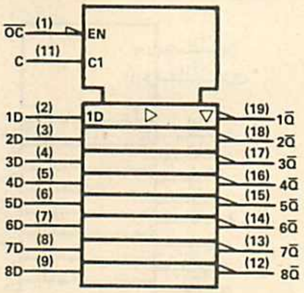
- Three-state buffer-type outputs drive bus lines directly

typical performance

TYPE	DELAY	TOTAL POWER
'ALS580	11 ns	67.5 mW
'AS580	5.5 ns	330 mW

SN54ALS580 (J,FH) SN74ALS580 (N,FN)
SN54AS580 (J,FH) SN74AS580 (N,FN)

logic symbol†


$\overline{\text{OC}}$ (1) EN
C (11) C1
1D (2) 1D
2D (3)
3D (4)
4D (5)
5D (6)
6D (7)
7D (8)
8D (9)
(19) $1\overline{\text{Q}}$
(18) $2\overline{\text{Q}}$
(17) $3\overline{\text{Q}}$
(16) $4\overline{\text{Q}}$
(15) $5\overline{\text{Q}}$
(14) $6\overline{\text{Q}}$
(13) $7\overline{\text{Q}}$
(12) $8\overline{\text{Q}}$

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{\text{OC}}$	11	C	1	$\overline{\text{OC}}$	11	C
2	1D	12	$8\overline{\text{Q}}$	2	1D	12	$8\overline{\text{Q}}$
3	2D	13	$7\overline{\text{Q}}$	3	2D	13	$7\overline{\text{Q}}$
4	3D	14	$6\overline{\text{Q}}$	4	3D	14	$6\overline{\text{Q}}$
5	4D	15	$5\overline{\text{Q}}$	5	4D	15	$5\overline{\text{Q}}$
6	5D	16	$4\overline{\text{Q}}$	6	5D	16	$4\overline{\text{Q}}$
7	6D	17	$3\overline{\text{Q}}$	7	6D	17	$3\overline{\text{Q}}$
8	7D	18	$2\overline{\text{Q}}$	8	7D	18	$2\overline{\text{Q}}$
9	8D	19	$1\overline{\text{Q}}$	9	8D	19	$1\overline{\text{Q}}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

590, 591

8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

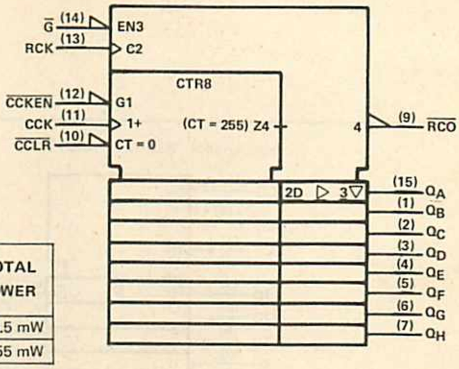
- 'LS590 has three-state register outputs
- 'LS591 has open-collector register outputs
- Counter has direct clear

typical performance

TYPE	MAX COUNT FREQ	PARALLEL LOAD	CLEAR	TOTAL POWER
'LS590	20 MHz	SYNC	SYNC-L	166.5 mW
'LS591	20 MHz	SYNC	SYNC-L	155 mW

SN54LS590 (J,FH) SN74LS590 (J,N,FN)
SN54LS591 (J,FH) SN74LS591 (J,N,FN)

logic symbol, 'LS590†

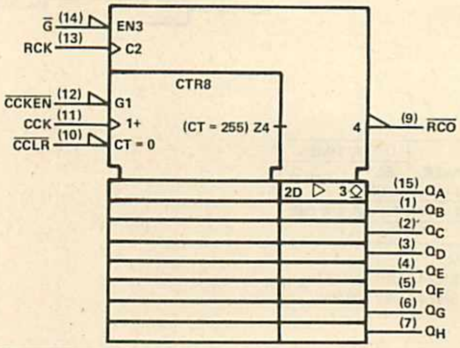

$\overline{\text{G}}$ (14) EN3
RCK (13) C2
CTR8
$\overline{\text{CCKEN}}$ (12) G1
CCK (11) 1+
$\overline{\text{CCLR}}$ (10) CT = 0
(CT = 255) Z4
4
(9) $\overline{\text{RCO}}$
2D
3
(15) Q_A
(1) Q_B
(2) Q_C
(3) Q_D
(4) Q_E
(5) Q_F
(6) Q_G
(7) Q_H

pin assignments

J, N PACKAGES			
1	Q_B	9	$\overline{\text{RCO}}$
2	Q_C	10	$\overline{\text{CCLR}}$
3	Q_D	11	CCK
4	Q_E	12	$\overline{\text{CCKEN}}$
5	Q_F	13	RCK
6	Q_G	14	$\overline{\text{G}}$
7	Q_H	15	Q_A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	Q_B	12	$\overline{\text{RCO}}$
3	Q_C	13	$\overline{\text{CCLR}}$
4	Q_D	14	CCK
5	Q_E	15	$\overline{\text{CCKEN}}$
6	nc	16	nc
7	Q_F	17	RCK
8	Q_G	18	$\overline{\text{G}}$
9	Q_H	19	Q_A
10	GND	20	V_{CC}

logic symbol, 'LS591†


$\overline{\text{G}}$ (14) EN3
RCK (13) C2
CTR8
$\overline{\text{CCKEN}}$ (12) G1
CCK (11) 1+
$\overline{\text{CCLR}}$ (10) CT = 0
(CT = 255) Z4
4
(9) $\overline{\text{RCO}}$
2D
3
(15) Q_A
(1) Q_B
(2) Q_C
(3) Q_D
(4) Q_E
(5) Q_F
(6) Q_G
(7) Q_H

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

589

8-BIT SHIFT REGISTERS WITH INPUT LATCHES

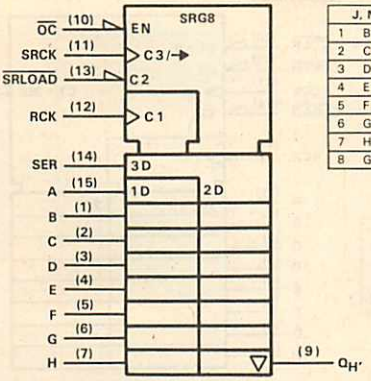
- 3-Step Outputs
- Has parallel storage register inputs
- Shift register has direct over-riding load
- Guaranteed shift frequency . . . dc to 20 MHz

typical performance

TYPE	SERIAL DATA INPUT	TOTAL POWER
'LS589	D	130 mW

SN54LS589 (J,FH) SN74LS589 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	B	9	$Q_{H'}$
2	C	10	$\overline{OC}$
3	D	11	SRCK
4	E	12	RCK
5	F	13	$\overline{SRLOAD}$
6	G	14	SER
7	H	15	A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	NC	11	NC
2	B	12	$Q_{H'}$
3	C	13	$\overline{OC}$
4	D	14	SRCK
5	E	15	RCK
6	NC	16	NC
7	F	17	$\overline{SRLOAD}$
8	G	18	SER
9	H	19	A
10	GND	20	V_{CC}

618

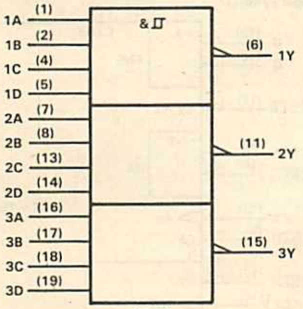
SCHMITT-TRIGGER POSITIVE-NAND GATES WITH TOTEM-POLE OUTPUTS

typical performances

TYPE	HYSTERESIS	DELAY
'LS618	0.7 V	25 ns

SN54LS618 (J,FH) SN74LS618 (J,N,FN)

logic symbol†



positive logic: Y = $\overline{ABCD}$

pin assignments

J, N PACKAGES			
1	1A	11	2Y
2	1B	12	NC
3	NC	13	2C
4	1C	14	2D
5	1D	15	3Y
6	1Y	16	3A
7	2A	17	3B
8	2B	18	3C
9	NC	19	3D
10	GND	2D	V_{CC}

FH, FN PACKAGES			
1	1A	11	2Y
2	1B	12	NC
3	NC	13	2C
4	1C	14	2D
5	1D	15	3Y
6	1Y	16	3A
7	2A	17	3B
8	2B	18	3C
9	NC	19	3D
10	GND	20	V_{CC}

619

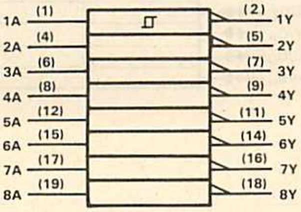
SCHMITT-TRIGGER INVERTERS WITH TOTEM-POLE OUTPUTS

typical performance

TYPE	HYSTERESIS	DELAY
'LS619	0.7 V	16 ns

SN54LS619 (J,FH) SN74LS619 (J,N,FN)

logic symbol†



positive logic: Y = $\overline{A}$

pin assignments

J, N PACKAGES			
1	1A	11	5Y
2	1Y	12	5A
3	NC	13	NC
4	2A	14	6Y
5	2Y	15	6A
6	3A	16	7Y
7	3Y	17	7A
8	4A	18	8Y
9	4Y	19	8A
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1A	11	5Y
2	1Y	12	5A
3	NC	13	NC
4	2A	14	6Y
5	2Y	15	6A
6	3A	16	7Y
7	3Y	17	7A
8	4A	18	8Y
9	4Y	19	8A
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

NC — No internal connection.

592

8-BIT BINARY COUNTERS WITH INPUT REGISTERS

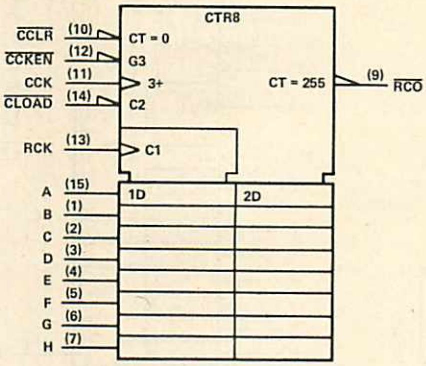
- Has parallel register inputs
- Counter has direct overriding load and clear
- Guaranteed counter frequency . . . dc to 20 MHz

typical performance

MAX COUNT FREQ	PARALLEL LOAD	CLEAR	TOTAL POWER
20 MHz	SYNC	SYNC-L	130 mW

SN54LS592 (J,FH)
SN74LS592 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	B	9	$\overline{RCO}$
2	C	10	$\overline{CCLR}$
3	D	11	CCK
4	E	12	$\overline{CCKEN}$
5	F	13	RCK
6	G	14	$\overline{CLOAD}$
7	H	15	A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	B	12	$\overline{RCO}$
3	C	13	$\overline{CCLR}$
4	D	14	CCK
5	E	15	$\overline{CCKEN}$
6	nc	16	nc
7	F	17	RCK
8	G	18	$\overline{CLOAD}$
9	H	19	A
10	GND	20	V_{CC}

593

8-BIT BINARY COUNTERS WITH INPUT REGISTERS

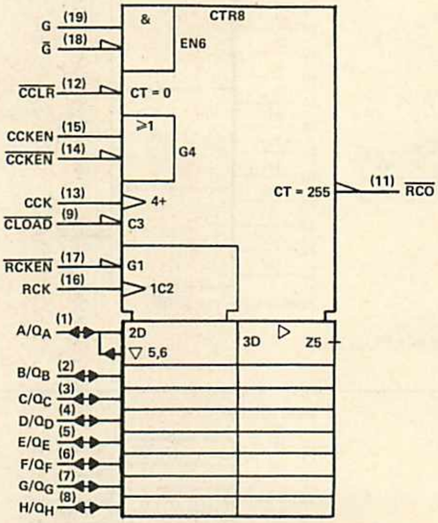
- Has parallel three-state I/O: register inputs/counter outputs
- Counter has direct overriding load and clear
- Guaranteed counter frequency . . . dc to 20 MHz

typical performance

MAX COUNT FREQ	PARALLEL LOAD	CLEAR	TOTAL POWER
20 MHz	SYNC	SYNC-L	177 mW

SN54LS593 (J,FH)
SN74LS593 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	A/Q_A	11	$\overline{RCO}$
2	B/Q_B	12	$\overline{CCLR}$
3	C/Q_C	13	CCK
4	D/Q_D	14	$\overline{CCKEN}$
5	E/Q_E	15	CCKEN
6	F/Q_F	16	RCK
7	G/Q_G	17	$\overline{RCKEN}$
8	H/Q_H	18	$\overline{G}$
9	$\overline{CLOAD}$	19	G
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	A/Q_A	11	$\overline{RCO}$
2	B/Q_B	12	$\overline{CCLR}$
3	C/Q_C	13	CCK
4	D/Q_D	14	$\overline{CCKEN}$
5	E/Q_E	15	CCKEN
6	F/Q_F	16	RCK
7	G/Q_G	17	$\overline{RCKEN}$
8	H/Q_H	18	$\overline{G}$
9	$\overline{CLOAD}$	19	G
10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

594

8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

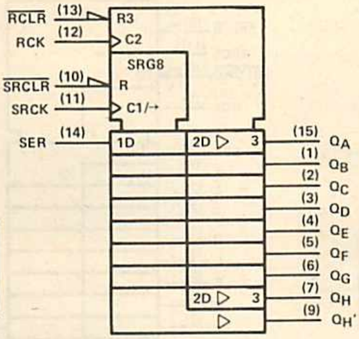
- Serial-in, parallel-out shift registers with storage
- Buffered outputs
- Guaranteed shift frequency . . . dc to 20 MHz

typical performance

TYPE	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'LS594	D	Low	180 mW

SN54LS594 (J,FH)   SN74LS594 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	Q_B	9	$Q_{H'}$
2	Q_C	10	$\overline{\text{SRCLR}}$
3	Q_D	11	SRCK
4	Q_E	12	RCK
5	Q_F	13	$\overline{\text{RCLR}}$
6	Q_G	14	SER
7	Q_H	15	Q_A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	Q_B	12	$Q_{H'}$
3	Q_C	13	$\overline{\text{SRCLR}}$
4	Q_D	14	SRCK
5	Q_E	15	RCK
6	nc	16	nc
7	Q_F	17	$\overline{\text{RCLR}}$
8	Q_G	18	SER
9	Q_H	19	Q_A
10	GND	20	V_{CC}

595, 596

8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

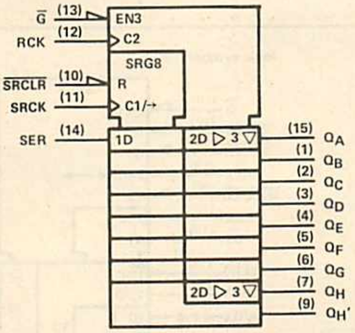
- Serial-in, parallel-out shift registers with storage
- 'LS595 has three-state parallel outputs
- 'LS596 has open-collector parallel outputs
- Guaranteed shift frequency . . . dc to 20 MHz

typical performance

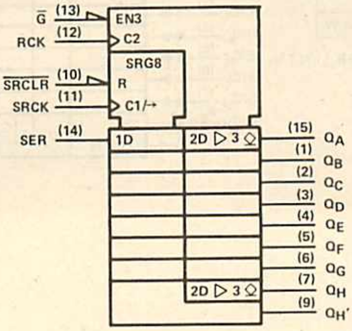
TYPE	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'LS595	D	LOW	167 mW
'LS596	D	LOW	160 mW

SN54LS595 (J,FH)   SN74LS595 (J,N,FN)
SN54LS596 (J,FH)   SN74LS596 (J,N,FN)

logic symbol, 'LS595†



logic symbol, 'LS596†



pin assignments

J, N PACKAGES			
1	Q_B	9	$Q_{H'}$
2	Q_C	10	$\overline{\text{SRCLR}}$
3	Q_D	11	$\overline{\text{SRCK}}$
4	Q_E	12	RCK
5	Q_F	13	$\overline{\text{G}}$
6	Q_G	14	SER
7	Q_H	15	Q_A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	Q_B	12	$Q_{H'}$
3	Q_C	13	$\overline{\text{SCLR}}$
4	Q_D	14	SCK
5	Q_E	15	RCK
6	nc	16	nc
7	Q_F	17	$\overline{\text{G}}$
8	Q_G	18	SER
9	Q_H	19	Q_A
10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

597

8-BIT SHIFT REGISTERS WITH INPUT LATCHES

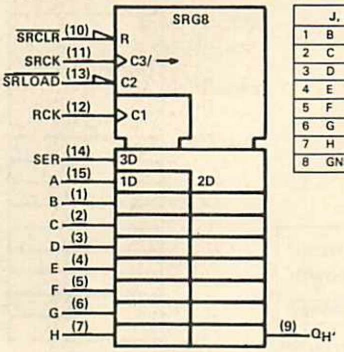
- Has parallel storage register inputs
- Shift register has direct overriding load and clear
- Guaranteed shift frequency . . . dc to 20 MHz

typical performance

TYPE	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'LS597	D	LOW	130 mW

SN54LS597 (J,FH) SN74LS597 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	B	9	$Q_{H'}$
2	C	10	$\overline{\text{SRCLR}}$
3	D	11	SRCK
4	E	12	RCK
5	F	13	$\overline{\text{SRLOAD}}$
6	G	14	SER
7	H	15	A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	B	12	$Q_{H'}$
3	C	13	$\overline{\text{SRCLR}}$
4	D	14	SRCK
5	E	15	RCK
6	nc	16	nc
7	F	17	$\overline{\text{SRLOAD}}$
8	G	18	SER
9	H	19	A
10	GND	20	V_{CC}

598

8-BIT SHIFT REGISTERS WITH INPUT LATCHES

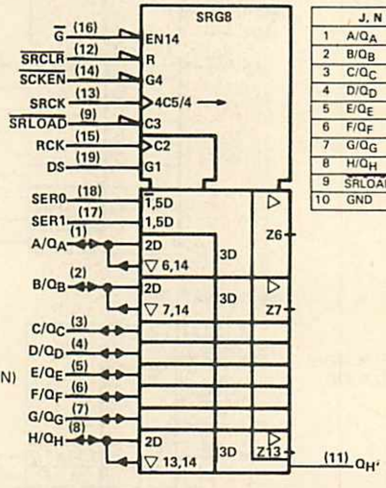
- Has parallel three-state I/O storage register inputs, shift register outputs
- Shift register has direct overriding load and clear
- Guaranteed shift frequency . . . dc to 20 MHz

typical performance

TYPE	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'LS598	D	LOW	177 mW

SN54LS598 (J,FH) SN74LS598 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	A/Q_A	11	$Q_{H'}$
2	B/Q_B	12	$\overline{\text{SRCLR}}$
3	C/Q_C	13	SRCK
4	D/Q_D	14	$\overline{\text{SRCKEN}}$
5	E/Q_E	15	RCK
6	F/Q_F	16	$\overline{\text{G}}$
7	G/Q_G	17	SER1
8	H/Q_H	18	SER0
9	$\overline{\text{SRLOAD}}$	19	DS
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	A/Q_A	11	$Q_{H'}$
2	B/Q_B	12	$\overline{\text{SRCLR}}$
3	C/Q_C	13	SRCK
4	D/Q_D	14	$\overline{\text{SCKEN}}$
5	E/Q_E	15	RCK
6	F/Q_F	16	$\overline{\text{G}}$
7	G/Q_G	17	SER1
8	H/Q_H	18	SER0
9	$\overline{\text{SRLOAD}}$	19	DS
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

599

8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

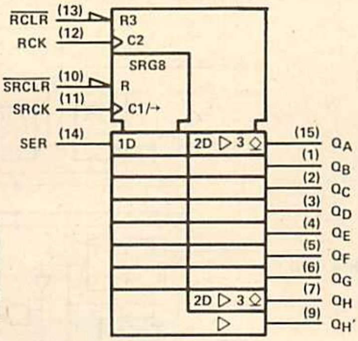
- Serial-in, parallel-out shift registers
- Open-collector outputs
- Guaranteed shift frequency . . . dc to 20 MHz

typical performance

TYPE	SERIAL DATA INPUT	ASYNC CLEAR	TOTAL POWER
'LS599	D	Low	170 mW

SN54LS599 (J,FH) SN74LS599 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	Q_B	9	$Q_{H'}$
2	Q_C	10	$\overline{\text{SRCLR}}$
3	Q_D	11	SRCK
4	Q_E	12	RCK
5	Q_F	13	$\overline{\text{RCLR}}$
6	Q_G	14	SER
7	Q_H	15	Q_A
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	Q_B	12	$Q_{H'}$
3	Q_C	13	$\overline{\text{SRCLR}}$
4	Q_D	14	SRCK
5	Q_E	15	RCK
6	nc	16	nc
7	Q_F	17	$\overline{\text{RCLR}}$
8	Q_G	18	SER
9	Q_H	19	Q_A
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

600

MEMORY REFRESH CONTROLLERS

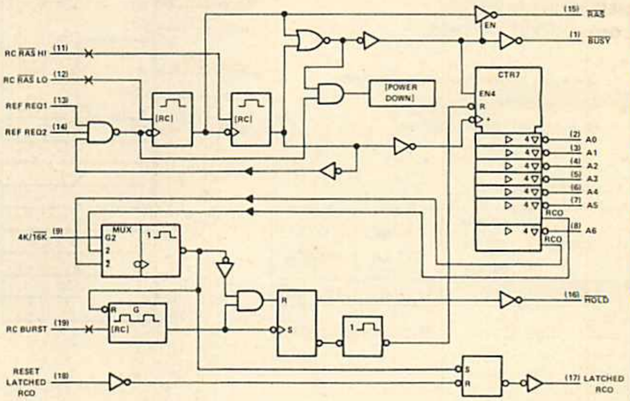
- Controls refresh cycle of 4K or 16K dynamic RAM's
- Three-state outputs drive bus lines directly
- Time to initiate refresh request is typically 30 ns
- Refresh modes: transparent, burst

SN74LS600A (J,N)

pin assignments

J,N PACKAGES			
1	$\overline{\mathrm{BUSY}}$	11	RC $\overline{\mathrm{RAS}}$ HI
2	A0	12	RC $\overline{\mathrm{RAS}}$ LO
3	A1	13	REF REQ1
4	A2	14	REF REQ2
5	A3	15	$\overline{\mathrm{RAS}}$
6	A4	16	$\overline{\mathrm{HOLD}}$
7	A5	17	LATCHED RCO
8	A6	18	RESET LATCHED RCO
9	4K/$\overline{\mathrm{16K}}$	19	RC BURST
10	GND	20	V_{CC}

logic diagram†



For chip carrier information, contact the factory.

601

MEMORY REFRESH CONTROLLERS

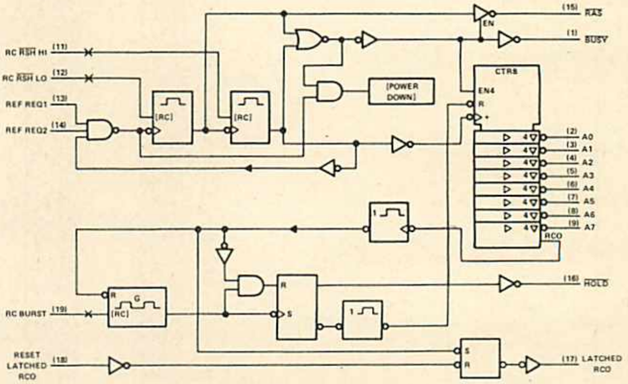
- Controls refresh cycle of 64K dynamic RAM's
- Three-state outputs drive bus lines directly
- Time to initiate refresh request is typically 30 ns
- Refresh modes: transparent, burst

SN74LS601A (J,N)

pin assignments

J,N PACKAGES			
1	$\overline{\mathrm{BUSY}}$	11	RC $\overline{\mathrm{RAS}}$ HI
2	A0	12	RC $\overline{\mathrm{RAS}}$ LO
3	A1	13	REF REQ1
4	A2	14	REF REQ2
5	A3	15	$\overline{\mathrm{RAS}}$
6	A4	16	$\overline{\mathrm{HOLD}}$
7	A5	17	LATCHED RCO
8	A6	18	RESET LATCHED RCO
9	A7	19	RC BURST
10	GND	20	V_{CC}

logic diagram†



For chip carrier information, contact the factory.

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†Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

602

MEMORY REFRESH CONTROLLERS

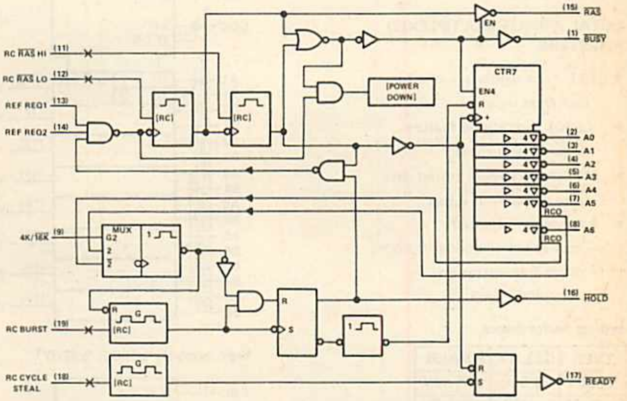
- Controls refresh cycle of 4K or 16K dynamic RAM's
- Three-state outputs drive bus lines directly
- Time to initiate refresh request is typically 30 ns
- Refresh modes: cycle steal, burst

SN74LS602A (J,N)

pin assignments

J, N PACKAGES			
1	$\overline{\text{BUSY}}$	11	RC $\overline{\text{RAS}}$ HI
2	A0	12	RC $\overline{\text{RAS}}$ LO
3	A1	13	REF REQ1
4	A2	14	REF REQ2
5	A3	15	$\overline{\text{RAS}}$
6	A4	16	$\overline{\text{HOLD}}$
7	A5	17	READY
8	A6	18	RC CYCLE STEAL
9	4K/16K	19	RC BURST
10	GND	20	V_{CC}

logic diagram†



For chip carrier information, contact the factory.

603

MEMORY REFRESH CONTROLLERS

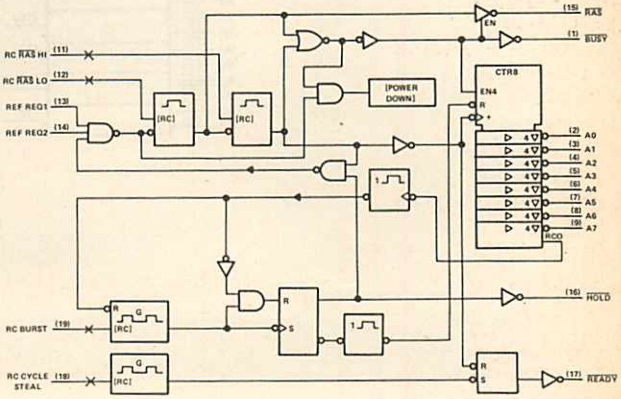
- Controls refresh cycle of 64K dynamic RAM's
- Three-state outputs drive bus lines directly
- Time to initiate refresh request is typically 30 ns
- Refresh modes: cycle steal, burst

SN74LS603A (J,N)

pin assignments

J, N PACKAGES			
1	$\overline{\text{BUSY}}$	11	RC $\overline{\text{RAS}}$ HI
2	A0	12	RC $\overline{\text{RAS}}$ LO
3	A1	13	REF REQ1
4	A2	14	REF REQ2
5	A3	15	$\overline{\text{RAS}}$
6	A4	16	$\overline{\text{HOLD}}$
7	A5	17	$\overline{\text{READY}}$
8	A6	18	RC CYCLE STEAL
9	A7	19	RC BURST
10	GND	20	V_{CC}

logic diagram†



For chip carrier information, contact the factory.

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†Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

604, 605
606, 607

OCTAL 2-INPUT MULTIPLEXED REGISTERS

- 16 D-type registers – one for each data input
- 'LS604 and 'LS606 feature three-state outputs
- Multiplexers select stored data from either A or B bus
- Application-oriented:
  - – max speed - ('LS604, 'LS605)
  - – glitch-free operation - ('LS606, 'LS607)

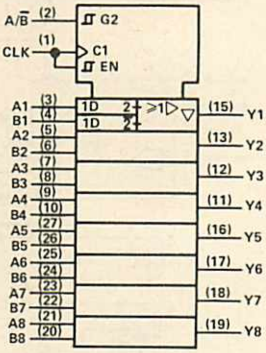
typical performance

TYPE	DELAY	POWER
'LS604	23.5 ns	275 mW
'LS605	26 ns	200 mW
'LS606	31 ns	275 mW
'LS607	31 ns	200 mW

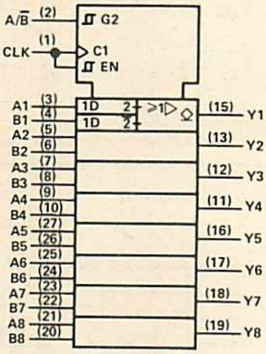
SN54LS604 (JD,FH)
SN54LS605 (JD,FH)
SN54LS606 (JD,FH)
SN54LS607 (JD,FH)

SN74LS604 (JD,N,FN)
SN74LS605 (JD,N,FN)
SN74LS606 (JD,N,FN)
SN74LS607 (JD,N,FN)

logic symbol, 'LS604, 'LS606†



logic symbol, 'LS605, 'LS607†



pin assignments

JD, N PACKAGES				FH, FN PACKAGES			
1	CLK	15	Y1	1	CLK	15	Y1
2	A/$\overline{B}$	16	Y5	2	A/$\overline{B}$	16	Y5
3	A1	17	Y6	3	A1	17	Y6
4	B1	18	Y7	4	B1	18	Y7
5	A2	19	Y8	5	A2	19	Y8
6	B2	20	B8	6	B2	20	B8
7	A3	21	A8	7	A3	21	A8
8	B3	22	B7	8	B3	22	B7
9	A4	23	A7	9	A4	23	A7
10	B4	24	B6	10	B4	24	B6
11	Y4	25	A6	11	Y4	25	A6
12	Y3	26	B5	12	Y3	26	B5
13	Y2	27	A5	13	Y2	27	A5
14	GND	28	V_{CC}	14	GND	28	V_{CC}

---

†Pin numbers shown on logic symbols are for JD and N packages only.

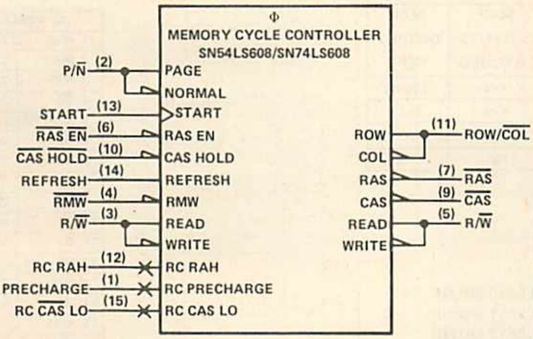
608

MEMORY CYCLE CONTROLLERS

- Read cycle
- Write cycle
- Read, modify, write cycle
- RAS only refresh cycle
- Page or normal modes
- Stand-alone controller for CPU-to-memory interface

SN54LS608 (J,FH) SN74LS608 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	PRECHARGE	9	$\overline{\mathrm{CAS}}$
2	P/$\overline{\mathrm{N}}$	10	$\overline{\mathrm{CAS}}$ $\overline{\mathrm{HOLD}}$
3	R/$\overline{\mathrm{W}}$ in	11	ROW/$\overline{\mathrm{COL}}$
4	$\overline{\mathrm{RMW}}$	12	RC RAH
5	R/$\overline{\mathrm{W}}$ out	13	START
6	$\overline{\mathrm{RAS}}$ $\overline{\mathrm{EN}}$	14	REFRESH
7	$\overline{\mathrm{RAS}}$	15	RC $\overline{\mathrm{CAS}}$ LO
8	GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	PRECHARGE	12	$\overline{\mathrm{CAS}}$
3	P/$\overline{\mathrm{N}}$	13	$\overline{\mathrm{CAS}}$ $\overline{\mathrm{HOLD}}$
4	R/$\overline{\mathrm{W}}$ in	14	ROW/$\overline{\mathrm{COL}}$
5	$\overline{\mathrm{RMW}}$	15	RC RAH
6	nc	16	nc
7	R/$\overline{\mathrm{W}}$ out	17	START
8	$\overline{\mathrm{RAS}}$ $\overline{\mathrm{EN}}$	18	REFRESH
9	$\overline{\mathrm{RAS}}$	19	RC $\overline{\mathrm{CAS}}$ LO
10	GND	20	V_{CC}

---

†Pin numbers shown on logic symbols are for J and N packages only.

610, 611 612, 613

MEMORY MAPPERS

typical performance

TYPE	MAP OUTPUTS LATCHED	MAP OUTPUT TYPE
'LS610	Yes	3-State
'LS611	Yes	O-C
'LS612	No	3-State
'LS613	No	O-C

- Designed for paged memory mapping
- Expands four address lines to 12 address lines

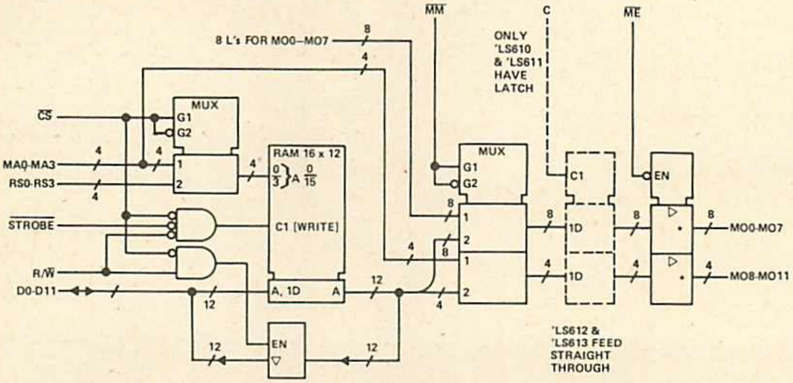
SN54LS610 (JD,FC)	SN74LS610 (JD,N)
SN54LS611 (JD,FC)	SN74LS611 (JD,N)
SN54LS612 (JD,FC)	SN74LS612 (JD,N)
SN54LS613 (JD,FC)	SN74LS613 (JD,N)

pin assignments

JD, N PACKAGES		FC PACKAGE	
1 RS2	21 $\overline{ME}$	1 RS2	23 $\overline{ME}$
2 MA3	22 MO6	2 MA3	24 MO6
3 RS3	23 MO7	3 RS3	25 MO7
4 $\overline{CS}$	24 MO8	4 $\overline{CS}$	26 MO8
5 $\overline{STROBE}$	25 MO9	5 $\overline{STROBE}$	27 MO9
6 R/$\overline{W}$	26 MO10	6 nc	28 nc
7 D0	27 MO11	7 R/$\overline{W}$	29 MO10
8 D1	28 ★	8 D0	30 MO11
9 D2	29 D6	9 D1	31 ★
10 D3	30 D7	10 D2	32 D6
11 D4	31 D8	11 D3	33 D7
12 D5	32 D9	12 D4	34 D8
13 $\overline{MM}$	33 D10	13 D5	35 D9
14 MO0	34 D11	14 $\overline{MM}$	36 D10
15 MO1	35 MA0	15 MO0	37 D11
16 MO2	36 RS0	16 MO1	38 MA0
17 MO3	37 MA1	17 nc	39 nc
18 MO4	38 RS1	18 MO2	40 RS0
19 MO5	39 MA2	19 MO3	41 MA1
20 GND	40 V_{CC}	20 MO4	42 RS1
		21 MO5	43 MA2
		22 GND	44 V_{CC}

★ C on 'LS610 and 'LS611
nc on 'LS612 and 'LS613

functional block diagram (positive logic)



*'LS610 and 'LS612 have 3-state (▽) map outputs.
'LS611 and 'LS613 have open-collector (⌂) map outputs.

nc — no internal connection.

620, 621
622, 623

OCTAL BUS TRANSCEIVERS

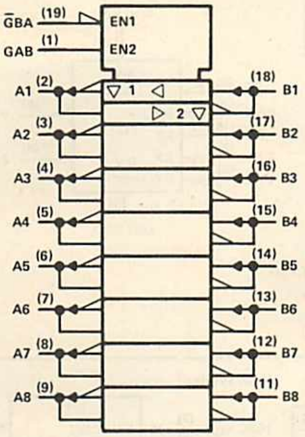
- Bidirectional bus transceivers
- Local bus latch capability

typical performance

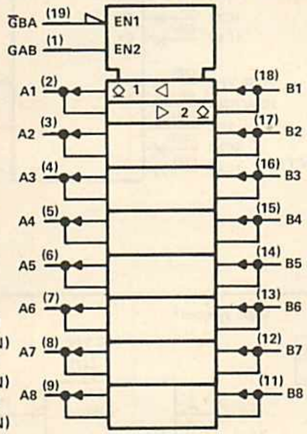
TYPE	OUTPUT	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS620A	3-State	– 12 mA	12 mA
SN74ALS620A	3-State	– 15 mA	24 mA
SN74ALS620A-1	3-State	– 15 mA	48 mA
SN54ALS621A	O-C	–	12 mA
SN74ALS621A	O-C	–	24 mA
SN74ALS621A-1	O-C	–	48 mA
SN54ALS622A	O-C	–	12 mA
SN74ALS622A	O-C	–	24 mA
SN74ALS622A-1	O-C	–	48 mA
SN54ALS623A	3-State	– 12 mA	12 mA
SN74ALS623A	3-State	– 15 mA	24 mA
SN74ALS623A-1	3-State	– 15 mA	48 mA
SN54AS620	3-State	– 12 mA	48 mA
SN74AS620	3-State	– 15 mA	64 mA
SN54AS621	O-C	–	48 mA
SN74AS621	O-C	–	64 mA
SN54AS622	O-C	–	48 mA
SN74AS622	O-C	–	64 mA
SN54AS623	3-State	– 12 mA	48 mA
SN74AS623	3-State	– 15 mA	64 mA
SN54LS620	3-State	– 12 mA	12 mA
SN74LS620	3-State	– 15 mA	24 mA
SN54LS621	O-C	–	12 mA
SN74LS621	O-C	–	24 mA
SN54LS622	O-C	–	12 mA
SN74LS622	O-C	–	24 mA
SN54LS623	3-State	– 12 mA	12 mA
SN74LS623	3-State	– 15 mA	24 mA

SN54ALS620A (J,FH)	SN74ALS620A, (N,FN) SN74ALS620A-1 (N,FN)
SN54ALS621A (J,FH)	SN74ALS621A (N,FN) SN74ALS621A-1 (N,FN)
SN54ALS622A (J,FH)	SN74ALS622A (N,FN) SN74ALS622A-1 (N,FN)
SN54ALS623A (J,FH)	SN74ALS623A (N,FN) SN74ALS623A-1 (N,FN)
SN54AS620 (J,FH)	SN74AS620 (N,FN)
SN54AS621 (J,FH)	SN74AS621 (N,FN)
SN54AS622 (J,FH)	SN74AS622 (N,FN)
SN54AS623 (J,FH)	SN74AS623 (N,FN)
SN54ALS620 (J,FH)	SN74ALS620 (J,N,FN)
SN54LS621 (J,FH)	SN74LS621 (J,N,FN)
SN54LS622 (j,FH)	SN74LS622 (J,N,FN)
SN54LS623 (J,FH)	SN74LS623 (J,N,FN)

logic symbol, 'ALS620A, AS620, 'LS620†



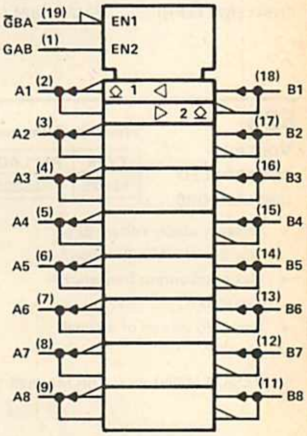
logic symbol, 'ALS621A, 'AS621, 'LS621†



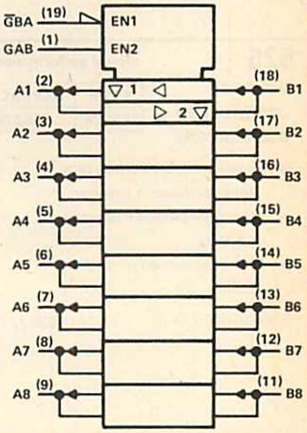
pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	GAB	11	B8	1	GAB	11	B8
2	A1	12	B7	2	A1	12	B7
3	A2	13	B6	3	A2	13	B6
4	A3	14	B5	4	A3	14	B5
5	A4	15	B4	5	A4	15	B4
6	A5	16	B3	6	A5	16	B3
7	A6	17	B2	7	A6	17	B2
8	A7	18	B1	8	A7	18	B1
9	A8	19	$\overline{G}BA$	9	A8	19	$\overline{G}BA$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol, 'ALS622A, 'AS622, 'LS622†



logic symbol, 'ALS623A, 'AS623, 'LS623†



† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

624

VOLTAGE-CONTROLLED OSCILLATORS

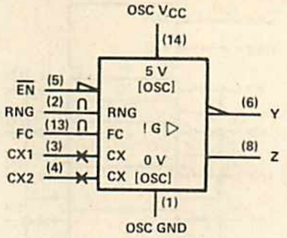
typical performance

TYPE	REPLACES
'LS624	'LS324

- Separate supply voltage pins for isolation of input/output signals
- Maximum output frequency = 20 MHz
- Improved version of original VCO family

SN54LS624 (J,FH) SN74LS624 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	OSC GND	8	Z
2	RNG	9	V_{CC}
3	CX1	10	nc
4	CX2	11	nc
5	$\overline{\text{EN}}$	12	nc
6	Y	13	FREQ CONT
7	GND	14	OSC V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	OSC GND	12	Z
3	RNG	13	V_{CC}
4	CX1	14	nc
5	nc	15	nc
6	CX2	16	nc
7	nc	17	nc
8	$\overline{\text{EN}}$	18	nc
9	Y	19	FREQ CONT
10	GND	20	OSC V_{CC}

625

VOLTAGE-CONTROLLED OSCILLATORS

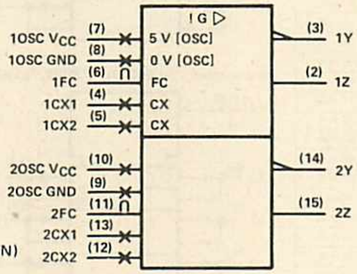
typical performance

TYPE	REPLACES
'LS625	'LS325

- Separate supply voltage pins for input/output isolation
- Maximum output frequency = 20 MHz
- Improved version of original family

SN54LS625 (J,FH) SN74LS625 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	GND	9	2OSC GND
2	1Z	10	2OSC V_{CC}
3	1Y	11	2FC
4	1CX1	12	2CX2
5	1CX2	13	2CX1
6	1FC	14	2Y
7	1OSC V_{CC}	15	2Z
8	1OSC GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	GND	12	2OSC GND
3	1Z	13	2OSC V_{CC}
4	1Y	14	2FC
5	1CX1	15	2CX2
6	nc	16	nc
7	1CX2	17	2CX1
8	1FC	18	2Y
9	1OSC V_{CC}	19	2Z
10	1OSC GND	20	V_{CC}

626

VOLTAGE-CONTROLLED OSCILLATORS

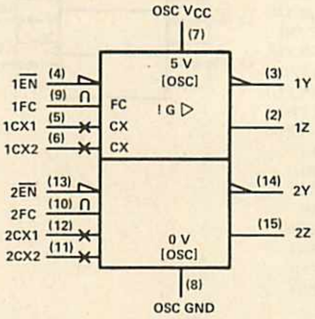
typical performance

TYPE	REPLACES
'LS626	'LS326

- Separate supply voltage pins for input/output isolation
- Maximum output frequency = 20 MHz
- Improved version of original family

SN54LS626 (J,FH) SN74LS626 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	GND	9	1FC
2	1Z	10	2FC
3	1Y	11	2CX2
4	1$\overline{\text{EN}}$	12	2CX1
5	1CX1	13	2$\overline{\text{EN}}$
6	1CX2	14	2Y
7	OSC V_{CC}	15	2Z
8	OSC GND	16	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	GND	12	1FC
3	1Z	13	2FC
4	1Y	14	2CX2
5	1$\overline{\text{EN}}$	15	2CX1
6	nc	16	nc
7	1CX1	17	2$\overline{\text{EN}}$
8	1CX2	18	2Y
9	OSC V_{CC}	19	2Z
10	OSC GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

627

VOLTAGE-CONTROLLED OSCILLATORS

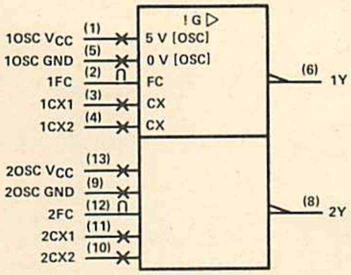
typical performance

TYPE	REPLACES
'LS627	'LS327

- Separate supply voltage pins for input/output isolation
- Maximum output frequency = 20 MHz
- Improved version of original family

SN54LS627 (J,FH)
SN74LS627 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1OSC V_{CC}	8	2Y	1	nc	11	nc
2	1FC	9	2OSC GND	2	1OSC V_{CC}	12	2Y
3	1CX1	10	2CX2	3	1FC	13	2OSC GND
4	1CX2	11	2CX1	4	1CX1	14	2CX2
5	1OSC GND	12	2FC	5	nc	15	nc
6	1Y	13	2OSC V_{CC}	6	1CX2	16	2CX1
7	GND	14	V_{CC}	7	nc	17	nc
				8	1OSC GND	18	2FC
				9	1Y	19	2OSC V_{CC}
				10	GND	20	V_{CC}

628

VOLTAGE-CONTROLLED OSCILLATORS

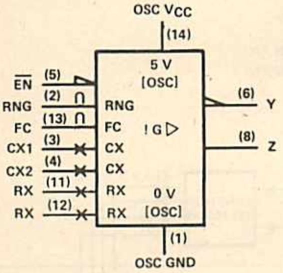
typical performance

TYPE	REPLACES
'LS628	'LS324

- Separate supply voltage pins for input/output oscillators
- Maximum output frequency = 20 MHz
- Improved version of original family

SN54LS628 (J,FH)
SN74LS628 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	OSC GND	8	Z	1	nc	11	nc
2	RNG	9	V_{CC}	2	OSC GND	12	Z
3	CX1	10	nc	3	RNG	13	V_{CC}
4	CX2	11	RX	4	CX1	14	nc
5	$\overline{EN}$	12	RX	5	nc	15	nc
6	Y	13	FC	6	CX2	16	RX
7	GND	14	OSC V_{CC}	7	nc	17	nc
				8	$\overline{EN}$	18	RX
				9	Y	19	FC
				10	GND	20	OSC V_{CC}

629

VOLTAGE-CONTROLLED OSCILLATORS

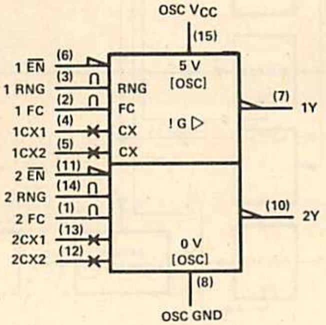
typical performance

TYPE	REPLACES
'LS629	'LS124

- Separate power supply pins for input/output isolation
- Maximum output frequency = 20 MHz
- Improved version of original family

SN54LS629 (J,FH)
SN74LS629 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	2FC	9	GND	1	nc	11	nc
2	1FC	10	2Y	2	2FC	12	GND
3	1RNG	11	2$\overline{EN}$	3	1FC	13	2Y
4	1CX1	12	2CX1	4	1RNG	14	2$\overline{EN}$
5	1CX2	13	2CX2	5	1CX1	15	2CX1
6	1$\overline{EN}$	14	2RNG	6	nc	16	nc
7	1Y	15	OSC V_{CC}	7	1CX2	17	2CX2
8	OSC GND	16	V_{CC}	8	1$\overline{EN}$	18	2RNG
				9	1Y	19	OSC V_{CC}
				10	OSC GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

630, 631

16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

- Fast processing times:
  - Write cycle: generates check word in 45 ns typical
  - Read cycle: flags errors in 27 ns typical
- Detects and corrects single bit error
- Detects and flags dual-bit errors

typical performance

TYPE	OUTPUT	DELAY	POWER
'LS630	3-State	27 ns	715 mW
'LS631	O-C	28 ns	565 mW

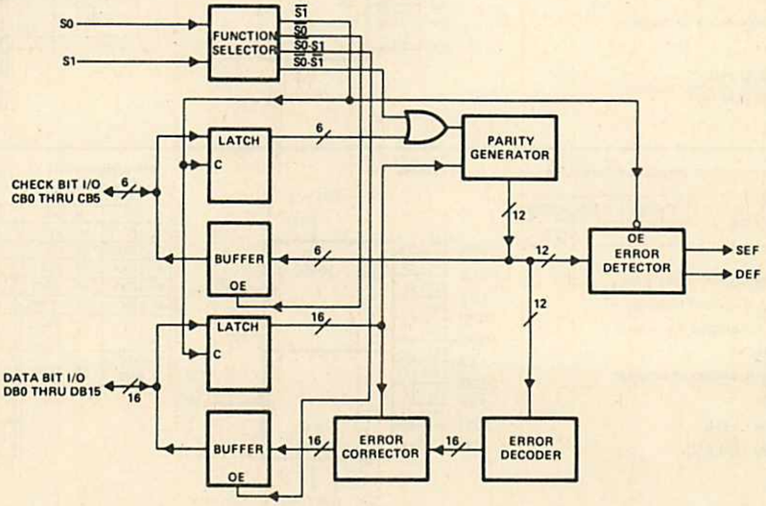
SN54LS630 (JD,FH)
SN54LS631 (JD,FH)

SN74LS630 (JD,N,FN)
SN74LS631 (JD,N,FN)

pin assignments

JD, N PACKAGES				FH, FN PACKAGES			
1	DEF	15	DB12	1	DEF	15	DB12
2	DB0	16	DB13	2	DB0	16	DB13
3	DB1	17	DB14	3	DB1	17	DB14
4	DB2	18	DB15	4	DB2	18	DB15
5	DB3	19	CB5	5	DB3	19	CB5
6	DB4	20	CB4	6	DB4	20	CB4
7	DB5	21	CB3	7	DB5	21	CB3
8	DB6	22	CB2	8	DB6	22	CB2
9	DB7	23	CB1	9	DB7	23	CB1
10	DB8	24	CB0	10	DB8	24	CB0
11	DB9	25	S0	11	DB9	25	S0
12	DB10	26	S1	12	DB10	26	S1
13	DB11	27	SEF	13	DB11	27	SEF
14	GND	28	V_{CC}	14	GND	28	V_{CC}

functional block diagram



nc — no internal connection.

632, 633

32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

- Detects and Corrects Single-bit errors
- Detects and Flags dual-bit errors
- Fast processing times
- Byte-Write capability

typical performance

TYPE	OUTPUT	DELAY	POWER
'ALS632	3-State		
'ALS633	O-C		

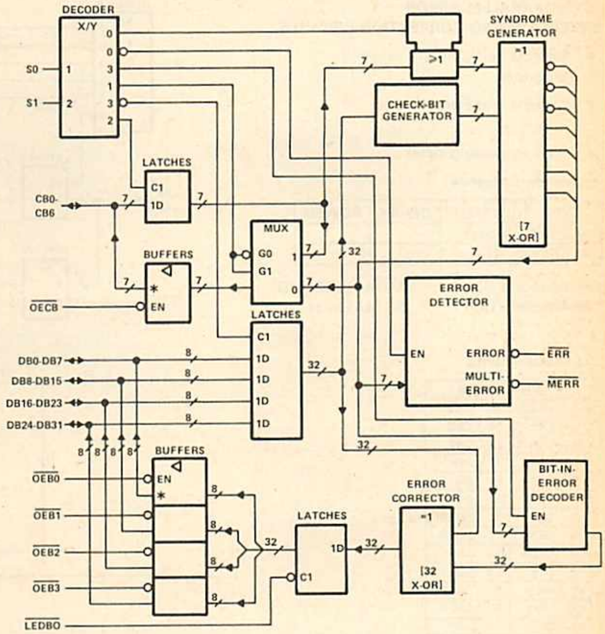
SN54ALS632 (JD) SN74ALS632 (JD)
SN54ALS633 (JD) SN74ALS633 (JD)

pin assignments

JD PACKAGE			
1	$\overline{\text{LEDBO}}$	27	CB3
2	$\overline{\text{MERR}}$	28	CB2
3	$\overline{\text{ERR}}$	29	CB1
4	DB0	30	CB0
5	DB1	31	DB16
6	DB2	32	DB17
7	DB3	33	DB18
8	DB4	34	DB19
9	DB5	35	DB20
10	$\overline{\text{OEB0}}$	36	DB21
11	DB6	37	$\overline{\text{OEB2}}$
12	DB7	38	DB22
13	GND	39	DB23
14	DB8	40	GND
15	DB9	41	DB24
16	$\overline{\text{OEB1}}$	42	DB25
17	DB10	43	$\overline{\text{OEB3}}$
18	DB11	44	DB26
19	DB12	45	DB27
20	DB13	46	DB28
21	DB14	47	DB29
22	DB15	48	DB30
23	CB6	49	DB31
24	CB5	50	S0
25	CB4	51	S1
26	$\overline{\text{OECB}}$	52	V_{CC}

For chip carrier information, contact the factory.

logic diagram (positive logic)



634, 635

32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

- Detects and Corrects single-bit errors
- Detects and Flags dual-bit errors
- Fast processing times

typical performance

TYPE	OUTPUT	DELAY	POWER
'ALS634	3-State		
'ALS635	O-C		

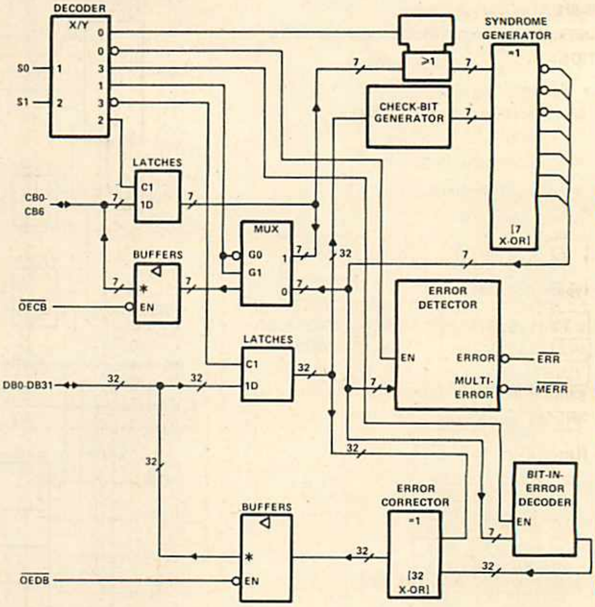
SN54ALS634 (JD) SN74ALS634 (JD)
SN54ALS635 (JD) SN74ALS635 (JD)

pin assignments

JD PACKAGES			
1	$\overline{\mathrm{MERR}}$	25	CB3
2	$\overline{\mathrm{ERR}}$	26	CB2
3	DB0	27	CB1
4	DB1	28	CB0
5	DB2	29	DB16
6	DB3	30	DB17
7	DB4	31	DB18
8	DB5	32	DB19
9	$\overline{\mathrm{OEDB}}$	33	DB20
10	DB6	34	DB21
11	DB7	35	DB22
12	GND	36	DB23
13	DB8	37	GND
14	DB9	38	DB24
15	DB10	39	DB25
16	DB11	40	DB26
17	DB12	41	DB27
18	DB13	42	DB28
19	DB14	43	DB29
20	DB15	44	DB30
21	CB6	45	DB31
22	CB5	46	S0
23	CB4	47	S1
24	$\overline{\mathrm{OECB}}$	48	V_{CC}

For chip carrier information, contact the factory.

logic diagram (positive logic)



636, 637

8-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

- Fast processing times:
  - Write cycle: generates check word in 45 ns typical
  - Read cycle: flags errors in 27 ns typical
- *Detects and corrects single bit error*
- Detects and flags dual-bit errors

typical performance

TYPE	OUTPUT	DELAY	POWER
'LS636	3-State	27 ns	500 mW
'LS637	O-C	28 ns	450 mW

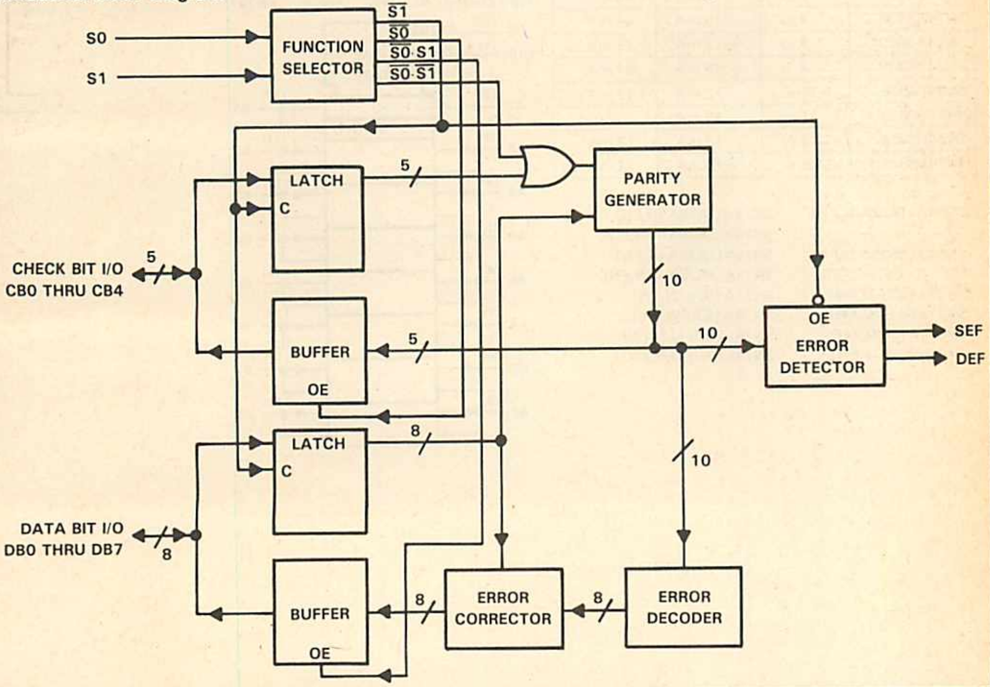
SN54LS636 (J) SN74LS636 (J,N)
SN54LS637 (J) SN74LS637 (J,N)

pin assignments

J, N PACKAGES			
1	DEF	11	CB4
2	DB0	12	nc
3	DB1	13	CB3
4	DB2	14	CB2
5	DB3	15	CB1
6	DB4	16	CB0
7	DB5	17	S0
8	DB6	18	S1
9	DB7	19	SEF
10	GND	20	V_{CC}

For chip carrier information, contact the factory.

functional block diagram



nc — no internal connection.

638, 639

OCTAL BUS TRANSCEIVERS

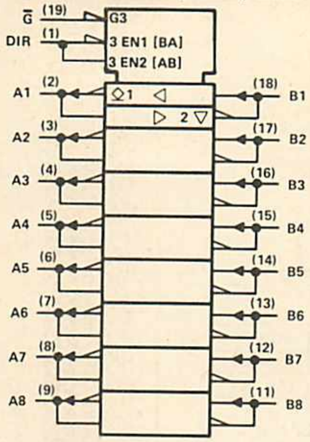
- Bidirectional bus transceivers
- "A" bus outputs are open-collector; "B" bus outputs are three-state
- 'ALS638, 'LS638 – inverting logic
- 'ALS639, 'LS639 – true logic

typical performance

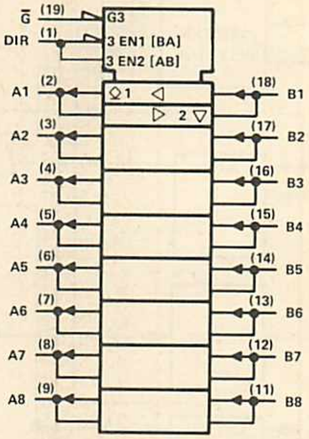
TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS638A	5 ns	– 12 mA	12 mA
SN74ALS638A	5 ns	– 15 mA	24 mA
SN74ALS638A-1	5 ns	– 15 mA	48 mA
SN54ALS639A	6 ns	– 12 mA	12 mA
SN74ALS639A	6 ns	– 15 mA	24 mA
SN74ALS639A-1	6 ns	– 15 mA	48 mA
SN54AS638	4 ns	– 12 mA	48 mA
SN74AS638	4 ns	– 15 mA	64 mA
SN54AS639	5 ns	– 12 mA	48 mA
SN74AS639	5 ns	– 15 mA	64 mA
SN54LS638	11 ns	– 12 mA	12 mA
SN74LS638	11 ns	– 15 mA	24 mA
SN54LS639	13.5 ns	– 12 mA	12 mA
SN74LS639	13.5 ns	– 15 mA	24 mA

SN54ALS638A (J,FH)	SN74ALS638A (N,FN)
	SN74ALS638A-1 (N,FN)
SN54ALS639A (J,FH)	SN74ALS639A (N,FN)
	SN74ALS639A-1 (N,FN)
SN54AS638 (J,FH)	SN74AS638 (N,FN)
SN54AS639 (J,FH)	SN74AS639 (N,FN)
SN54LS638 (J,FH)	SN74LS638 (J,N,FN)
SN54LS639 (J,FH)	SN74LS639 (J,N,FN)

logic symbol, 'ALS638A, 'AS638, 'LS638†



logic symbol, 'ALS639A, 'AS639, 'LS639†



pin assignments

J, N PACKAGES			
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{G}$
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{G}$
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

640, 641, 642
643, 644, 645

OCTAL BUS TRANSCEIVERS

TYPE	OUTPUT	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS640A	3-State	5 ns	− 12 mA	12 mA
SN74ALS640A	3-State	5 ns	− 15 mA	24 mA
SN74ALS640A-1	3-State	5 ns	− 15 mA	48 mA
SN54ALS641A	O-C	15 ns	N/A	12 mA
SN74ALS641A	O-C	15 ns	N/A	24 mA
SN74ALS641A-1	O-C	15 ns	N/A	48 mA
SN74ALS642A	O-C	20 ns	N/A	12 mA
SN54ALS642A	O-C	20 ns	N/A	24 mA
SN74ALS642A-1	O-C	20 ns	N/A	48 mA
SN54ALS643A	3-State	5 ns	− 12 mA	12 mA
SN74ALS643A	3-State	5 ns	− 15 mA	24 mA
SN74ALS643A-1	3-State	5 ns	− 15 mA	48 mA
SN54ALS644A	O-C	20 ns	N/A	12 mA
SN74ALS644A	O-C	20 ns	N/A	24 mA
SN74ALS644A-1	O-C	20 ns	N/A	48 mA
SN54ALS645A	3-State	6 ns	− 12 mA	12 mA
SN74ALS645A	3-State	6 ns	− 15 mA	24 mA
SN74ALS645A-1	3-State	6 ns	− 15 mA	48 mA
SN54AS640	3-State	4 ns	− 12 mA	48 mA
SN74AS640	3-State	4 ns	− 15 mA	64 mA
SN54AS641	O-C	20 ns	N/A	48 mA
SN74AS641	O-C	20 ns	N/A	64 mA
SN54AS642	O-C	20 ns	N/A	48 mA
SN74AS642	O-C	20 ns	N/A	64 mA
SN54AS643	3-State	4 ns	− 12 mA	48 mA
SN74AS643	3-State	4 ns	− 15 mA	64 mA
SN54AS644	O-C	20 ns	N/A	48 mA
SN74AS644	O-C	20 ns	N/A	64 mA
SN54AS645	3-State	5 ns	− 12 mA	48 mA
SN74AS645	3-State	5 ns	− 12 mA	64 mA
SN54LS640	3-State	7 ns	− 12 mA	12 mA
SN74LS640	3-State	7 ns	− 15 mA	24 mA
SN74LS640-1	3-State	7 ns	− 15 mA	48 mA
SN54LS641	O-C	16.5 ns	N/A	12 mA
SN74LS641	O-C	16.5 ns	N/A	24 mA
SN74LS641-1	O-C	16.5 ns	N/A	48 mA
SN54LS642	O-C	16.5 ns	N/A	12 mA
SN74LS642	O-C	16.5 ns	N/A	24 mA
SN74LS642-1	O-C	16.5 ns	N/A	48 mA
SN54LS643	3-State	8.5 ns	− 12 mA	12 mA
SN74LS643	3-State	8.5 ns	− 15 mA	24 mA
SN74LS643-1	3-State	8.5 ns	− 15 mA	48 mA
SN54LS644	O-C	16.5 ns	N/A	12 mA
SN74LS644	O-C	16.5 ns	N/A	24 mA
SN74LS644-1	O-C	16.5 ns	N/A	48 mA
SN54LS645	3-State	9.5 ns	− 12 mA	12 mA
SN74LS645	3-State	9.5 ns	− 15 mA	24 mA
SN74LS645-1	3-State	9.5 ns	− 15 mA	48 mA

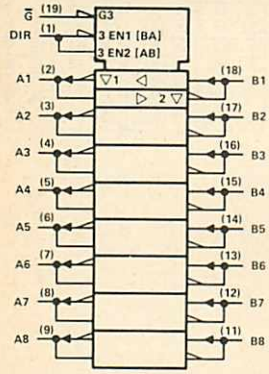
pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	DIR	11	B8	1	DIR	11	B8
2	A1	12	B7	2	A1	12	B7
3	A2	13	B6	3	A2	13	B6
4	A3	14	B5	4	A3	14	B5
5	A4	15	B4	5	A4	15	B4
6	A5	16	B3	6	A5	16	B3
7	A6	17	B2	7	A6	17	B2
8	A7	18	B1	8	A7	18	B1
9	A8	19	$\overline{G}$	9	A8	19	$\overline{G}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

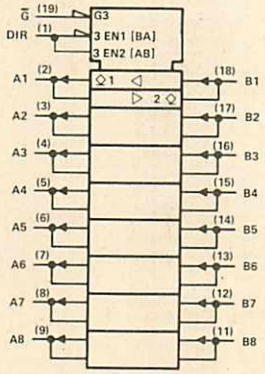
SN54ALS640A (J,FH)	SN74ALS640A (N,FN)	SN74ALS640A-1 (N,FN)
SN54ALS641A (J,FH)	SN74ALS641A (N,FN)	SN74ALS641A-1 (N,FN)
SN54ALS642A (J,FH)	SN74ALS642A (N,FN)	SN74ALS642A-1 (N,FN)
SN54ALS643A (J,FH)	SN74ALS643A (N,FN)	SN74ALS643A-1 (N,FN)
SN54ALS644A (J,FH)	SN74ALS644A (N,FN)	SN74ALS644A-1 (N,FN)
SN54ALS645A (J,FH)	SN74ASL645A (N,FN)	SN74ALS645A-1 (N,FN)
SN54AS640 (J,FH)	SN74AS640 (N,FN)	
SN54AS641 (J,FH)	SN74AS641 (N,FN)	
SN54AS642 (J,FH)	SN74AS642 (N,FN)	
SN54AS643 (J,FH)	SN74AS643 (N,FN)	
SN54AS644 (J,FH)	SN74AS644 (N,FN)	
SN54AS645 (J,FH)	SN74AS645 (N,FN)	
SN54LS640 (J,FH)	SN74LS640 (J,N,FN)	SN74LS640-1 (J,N,FN)
SN54LS641 (J,FH)	SN74LS641 (J,N,FN)	SN74LS641-1 (J,N,FN)
SN54LS642 (J,FH)	SN74LS642 (J,N,FN)	SN74LS642-1 (J,N,FN)
SN54LS643 (J,FH)	SN74LS643 (J,N,FN)	SN74LS643-1 (J,N,FN)
SN54LS644 (J,FH)	SN74LS644 (J,N,FN)	SN74LS644-1 (J,N,FN)
SN54LS645 (J,FH)	SN74LS645 (J,N,FN)	SN74LS645-1 (J,N,FN)

640, 641, 642
643, 644, 645 continued

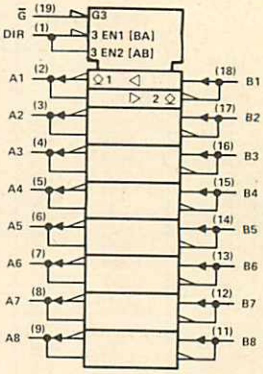
logic symbol, 'ALS640A, 'AS640, 'LS640†



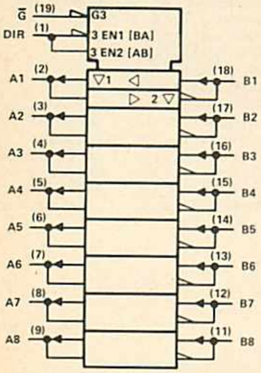
logic symbol, 'ALS641A, 'AS641, 'LS641†



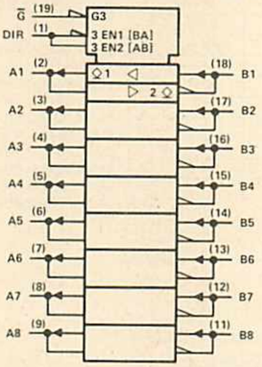
logic symbol, 'ALS642A, 'AS642, 'LS642†



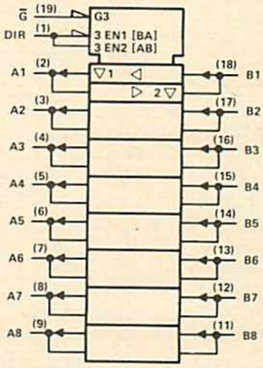
logic symbol, 'ALS643A, 'AS643, 'LS643†



logic symbol, 'ALS644A, 'AS644, 'LS644†



logic symbol, 'ALS645A, 'AS645, 'LS645†



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† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

646, 647, 648, 649

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bidirectional
- Independent registers for A and B busses

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	OUTPUT TYPE	OUTPUT INV
SN54ALS646		− 12 mA	12 mA	3-State	No
SN74ALS646		− 15 mA	24 mA	3-State	No
SN74ALS646-1		− 15 mA	48 mA	3-State	No
SN54ALS647		N/A	12 mA	O-C	No
SN74ALS647		N/A	24 mA	O-C	No
SN74ALS647-1		N/A	48 mA	O-C	No
SN54ALS648		− 12 mA	12 mA	3-State	Yes
SN74ALS648		− 15 mA	24 mA	3-State	Yes
SN74ALS648-1		− 15 mA	48 mA	3-State	Yes
SN54ALS649		N/A	12 mA	O-C	Yes
SN74ALS649		N/A	24 mA	O-C	Yes
SN74ALS649-1		N/A	48 mA	O-C	Yes
SN54AS646		− 12 mA	48 mA	3-State	No
SN74AS646		− 15 mA	64 mA	3-State	No
SN54AS648		− 12 mA	48 mA	3-State	Yes
SN74AS648		− 15 mA	64 mA	3-State	Yes
SN54LS646	19 ns	− 12 mA	12 mA	3-State	No
SN74LS646	19 ns	− 15 mA	24 mA	3-State	No
SN74LS647	25 ns	N/A	12 mA	O-C	No
SN74LS647	25 ns	N/A	24 mA	O-C	No
SN54LS648	20.5 ns	− 12 mA	12 mA	3-State	Yes
SN74LS648	20.5 ns	− 15 mA	24 mA	3-State	Yes
SN54LS649	25 ns	N/A	12 mA	O-C	Yes
SN74LS649	25 ns	N/A	24 mA	O-C	Yes

SN54ALS646 (JT, FH)	SN74ALS646 (NT,FN)
	SN74ALS646-1 (NT,FN)
SN54ALS647 (JT,FH)	SN74ALS647 (NT,FN)
	SN74ALS647-1 (NT,FN)
SN54ALS648 (JT,FH)	SN74ALS648 (NT,FN)
	SN74ALS648-1 (NT,FN)
SN54ALS649 (JT,FH)	SN74ALS649 (NT,FN)
	SN74ALS649-1 (NT,FN)
SN54AS646 (JT,FH)	SN74AS646 (NT,FN)
SN54AS648 (JT,FH)	SN74AS648 (NT,FN)
SN54LS646 (JT,FH)	SN74LS646 (JT,NT,FN)
SN54LS647 (JT,FH)	SN74LS647 (JT,NT,FN)
SN54LS648 (JT,FH)	SN74LS648 (JT,NT,FN)
SN54LS649 (JT,FH)	SN74LS649 (JT,NT,FN)

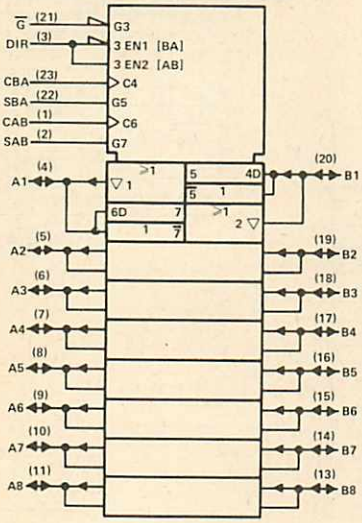
pin assignments

JT, NT PACKAGES			
1	CAB	13	B8
2	SAB	14	B7
3	DIR	15	B6
4	A1	16	B5
5	A2	17	B4
6	A3	18	B3
7	A4	19	B2
8	A5	20	B1
9	A6	21	$\overline{G}$
10	A7	22	SBA
11	A8	23	CBA
12	GND	24	V_{CC}

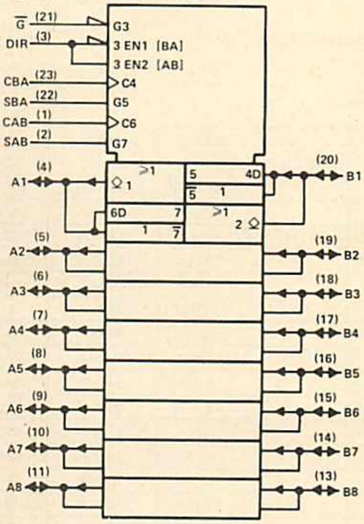
FH, FN PACKAGES			
1	nc	15	nc
2	CAB	16	B8
3	SAB	17	B7
4	DIR	18	B6
5	A1	19	B5
6	A2	20	B4
7	A3	21	B3
8	nc	22	nc
9	A4	23	B2
10	A5	24	B1
11	A6	25	$\overline{G}$
12	A7	26	SBA
13	A8	27	CBA
14	GND	28	V_{CC}

646, 647, 648, 649 continued

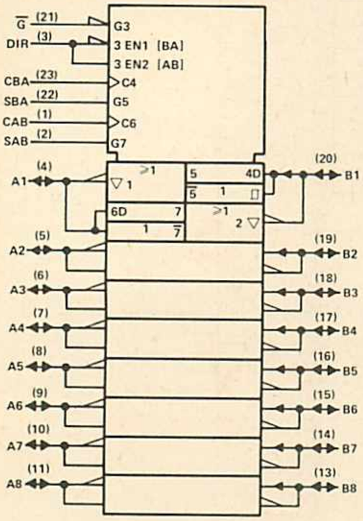
logic symbol, 'ALS646, 'AS646, 'LS646†



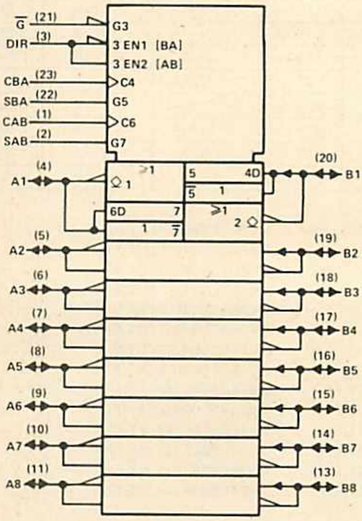
logic symbol, 'ALS647, 'LS647†



logic symbol, 'ALS648, 'AS648, 'LS648†



logic symbol, 'ALS649, 'LS649†



†Pin numbers shown on logic symbols are for JT and NT packages only.

nc — no internal connection.

651, 652

OCTAL BUS TRANSCEIVERS AND REGISTERS

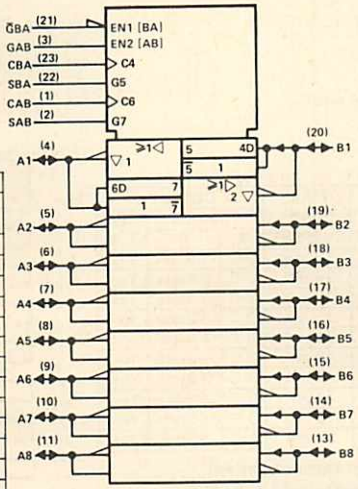
- Bidirectional
- Independent registers for A and B busses

typical performance

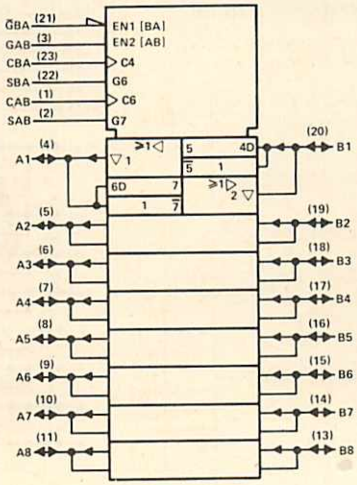
TYPE	MAX SOURCE CURRENT	MAX SINK CURRENT	OUTPUT TYPE A B	OUTPUT INV A,B
SN54ALS651	− 12 mA	12 mA	3-State	Yes
SN74ALS651	− 15 mA	24 mA	3-State	Yes
SN74ALS651-1	− 15 mA	48 mA	3-State	Yes
SN54ALS652	− 12 mA	12 mA	3-State	No
SN74ALS652	− 15 mA	24 mA	3-State	No
SN74ALS652-1	− 15 mA	48 mA	3-State	No
SN54AS651	− 12 mA	48 mA	3-State	Yes
SN74AS651	− 15 mA	64 mA	3-State	Yes
SN54AS652	− 12 mA	48 mA	3-State	No
SN74AS652	− 15 mA	64 mA	3-State	No
SN54LS651	− 12 mA	12 mA	3-State	Yes
SN74LS651	− 15 mA	24 mA	3-State	Yes
SN54LS652	− 12 mA	12 mA	3-State	No
SN74LS652	− 15 mA	24 mA	3-State	No

SN54ALS651 (JT,FH)	SN74ALS651 (NT,FN)
	SN74ALS651-1 (NT,FN)
SN54ALS652 (JT,FH)	SN74ALS652 (NT,FN)
	SN74ALS652-1 (NT,FN)
SN54AS651 (JT,FH)	SN74AS651 (NT,FN)
SN54AS652 (JT,FH)	SN74AS652 (NT,FN)
SN54LS651 (JT,FH)	SN74LS651 (JT,NT,FN)
SN54LS652 (JT,FH)	SN74LS652 (JT,NT,FN)

logic symbol, 'ALS651, 'AS651, 'LS651†



logic symbol, 'ALS652, 'AS652, 'LS652†



pin assignments

JT, NT PACKAGES			
1	CAB	13	B8
2	SAB	14	B7
3	GAB	15	B6
4	A1	16	B5
5	A2	17	B4
6	A3	18	B3
7	A4	19	B2
8	A5	20	B1
9	A6	21	$\overline{G}$BA
10	A7	22	SBA
11	A8	23	CBA
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	CAB	16	B8
3	SAB	17	B7
4	GAB	18	B6
5	A1	19	B5
6	A2	20	B4
7	A3	21	B3
8	nc	22	nc
9	A4	23	B2
10	A5	24	B1
11	A6	25	$\overline{G}$BA
12	A7	26	SBA
13	A8	27	CBA
14	GND	28	V_{CC}

†Pin numbers shown on logic symbols are for JT and NT packages only.

nc − no internal connection.

653, 654

OCTAL BUS TRANSCEIVERS AND REGISTERS

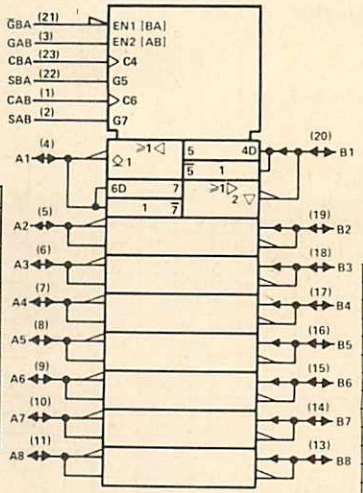
- Bidirectional
- Independent registers for A and B busses

typical performance

TYPE	MAX SOURCE CURRENT	MAX SINK CURRENT	OUTPUT TYPE		INV
			A	B	A, B
SN54ALS653	−12 mA	12 mA	O-C	3-State	Yes
SN74ALS653	−15 mA	24 mA	O-C	3-State	Yes
SN74ALS653-1	−15 mA	48 mA	O-C	3-State	Yes
SN54ALS654	−12 mA	12 mA	O-C	3-State	No
SN74ALS654	−15 mA	24 mA	O-C	3-State	No
SN74ALS654-1	−15 mA	48 mA	O-C	3-State	No
SN54LS653	−12 mA	12 mA	O-C	3-State	Yes
SN74LS653	−15 mA	24 mA	O-C	3-State	Yes
SN54LS654	−12 mA	12 mA	O-C	3-State	No
SN74LS654	−15 mA	24 mA	O-C	3-State	No

SN54ALS653 (JT,FH)	SN74ALS653 (NT,FN)
SN54ALS654 (JT,FH)	SN74ALS653-1 (NT,FN)
	SN74ALS654 (NT,FN)
	SN74ALS654-1 (NT,FN)
SN54LS653 (JT,FH)	SN74LS653 (JT,NT,FN)
SN54LS654 (JT,FH)	SN74LS654 (JT,NT,FN)

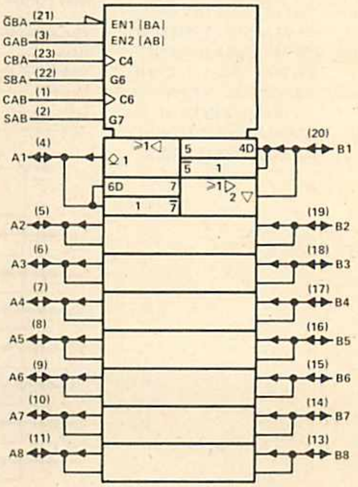
logic symbol, 'ALS653, 'LS653†



JT, NT PACKAGES			
1	CAB	13	B8
2	SAB	14	B7
3	GAB	15	B6
4	A1	16	B5
5	A2	17	B4
6	A3	18	B3
7	A4	19	B2
8	A5	20	B1
9	A6	21	$\overline{G}$BA
10	A7	22	SBA
11	A8	23	CBA
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	CAB	16	B8
3	SAB	17	B7
4	GAB	18	B6
5	A1	19	B5
6	A2	20	B4
7	A3	21	B3
8	nc	22	nc
9	A4	23	B2
10	A5	24	B1
11	A6	25	$\overline{G}$BA
12	A7	26	SBA
13	A8	27	CBA
14	GND	28	V_{CC}

logic symbol, 'ALS654, 'LS654†



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† Pin numbers shown on logic symbols are for JT and NT packages only.

nc – no internal connection.

668, 669

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

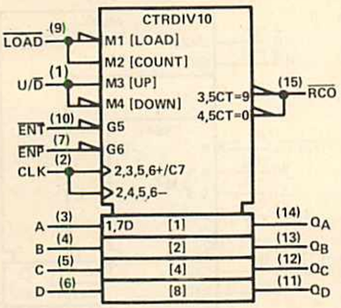
- Programmable, look-ahead
- Decade counter ('LS668)
- Binary counter ('LS669)

typical performance

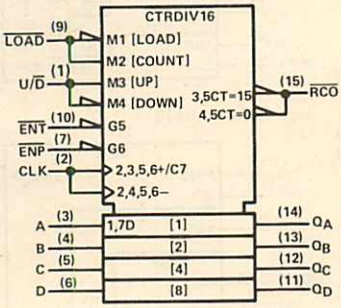
TYPE	COUNT FREQ	PARALLEL LOAD	TOTAL POWER
'LS668	32 MHz	Sync	100 mW
'LS669	32 MHz	Sync	100 mW

SN54LS668 (J,FH) SN74LS668 (J,N,FN)
SN54LS669 (J,FH) SN74LS669 (J,N,FN)

logic symbol, 'LS668†



logic symbol, 'LS669†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	U/$\overline{\text{D}}$	9	$\overline{\text{LOAD}}$	1	nc	11	nc
2	CLK	10	$\overline{\text{ENT}}$	2	U/$\overline{\text{D}}$	12	$\overline{\text{LOAD}}$
3	A	11	Q_D	3	CLK	13	$\overline{\text{ENT}}$
4	B	12	Q_C	4	A	14	Q_D
5	C	13	Q_B	5	B	15	Q_C
6	D	14	Q_A	6	nc	16	nc
7	$\overline{\text{ENP}}$	15	$\overline{\text{RCO}}$	7	C	17	Q_B
8	GND	16	V_{CC}	8	D	18	Q_A
				9	$\overline{\text{ENP}}$	19	$\overline{\text{RCO}}$
				10	GND	20	V_{CC}

670

4-BY-4 REGISTER FILES

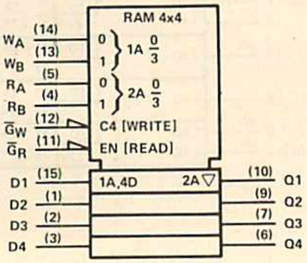
- 3-state outputs
- Simultaneous read/write
- Expandable to 1024 words

typical performance

ADDRESS TIME	ENABLE TIME	POWER/BIT
24 ns	19 ns	9.3 mW

SN54LS670 (J,FH) SN74LS670 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D2	9	Q2	1	nc	11	nc
2	D3	10	Q1	2	D2	12	Q2
3	D4	11	$\overline{G}_R$	3	D3	13	Q1
4	R_B	12	$\overline{G}_W$	4	D4	14	$\overline{G}_R$
5	R_A	13	W_B	5	R_B	15	$\overline{G}_W$
6	Q4	14	W_A	6	nc	16	nc
7	Q3	15	D1	7	R_A	17	W_B
8	GND	16	V_{CC}	8	Q4	18	W_A
				9	Q3	19	D1
				10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

671, 672

4-BIT UNIVERSAL SHIFT REGISTERS/LATCHES WITH THREE-STATE OUTPUTS

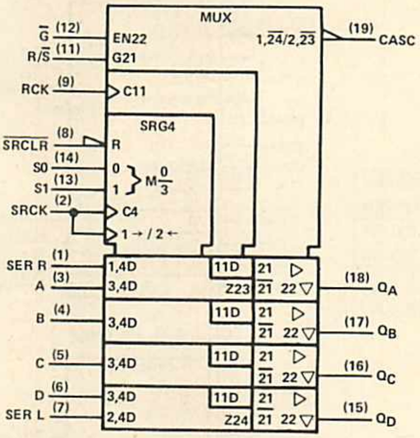
- '671 has direct SR clear
- '672 has synchronous SR clear
- Expandable to any word length
- Multiplexed outputs for shift register or latched data
- Four modes of shift register
  - Inhibit clock
  - Shift right
  - Shift left
  - Parallel load

typical performance

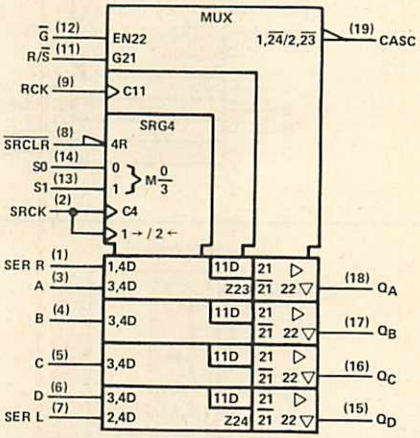
TYPE	TOTAL POWER
'LS671	170 mW
'LS672	170 mW

SN54LS671 (J,FH) SN74LS671 (J,N,FN)
SN54LS672 (J,FH) SN74LS672 (J,N,FN)

logic symbol, 'LS671†



logic symbol, 'LS672†



pin assignments

J, N PACKAGES			
1	SER R	11	$R/\overline{S}$
2	SRCK	12	$\overline{G}$
3	A	13	S1
4	B	14	S0
5	C	15	Q_D
6	D	16	Q_C
7	SER L	17	Q_B
8	$\overline{SRCLR}$	18	Q_A
9	RCK	19	CASC
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	SER R	11	$R/\overline{S}$
2	SRCK	12	$\overline{G}$
3	A	13	S1
4	B	14	S0
5	C	15	Q_D
6	D	16	Q_C
7	SER L	17	Q_B
8	$\overline{SRCLR}$	18	Q_A
9	RCK	19	CASC
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

673

16-BIT SHIFT REGISTERS

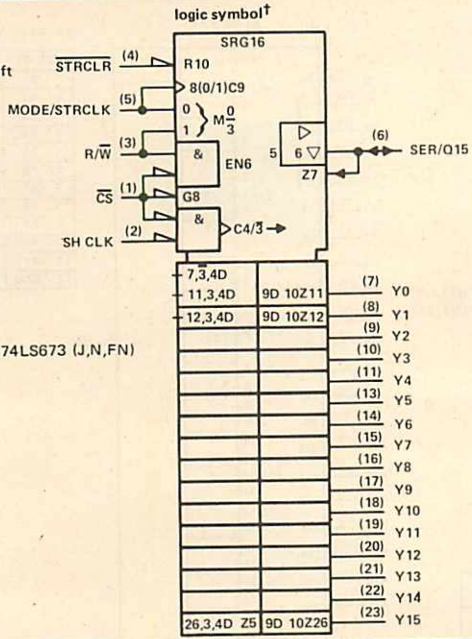
- 16-bit serial-in/serial-out shift register with three-state outputs
- 16-bit parallel-out storage register
- Converts serial to parallel data flow

typical performance

TYPE	SHIFT FREQ	TOTAL POWER
'LS673	20 MHz	255 mW

SN54LS673 (J,FH) SN74LS673 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{CS}$	13	Y5
2	SH CLK	14	Y6
3	R/$\overline{W}$	15	Y7
4	$\overline{STRCLR}$	16	Y8
5	MODE/STRCLR	17	Y9
6	SER/Q15	18	Y10
7	Y0	19	Y11
8	Y1	20	Y12
9	Y2	21	Y13
10	Y3	22	Y14
11	Y4	23	Y15
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{CS}$	16	Y5
3	SH CLK	17	Y6
4	R/$\overline{W}$	18	Y7
5	$\overline{STRCLR}$	19	Y8
6	MODE/STRCLR	20	Y9
7	SER/Q15	21	Y10
8	nc	22	nc
9	Y0	23	Y11
10	Y1	24	Y12
11	Y2	25	Y13
12	Y3	26	Y14
13	Y4	27	Y15
14	GND	28	V_{CC}

674

16-BIT SHIFT REGISTER

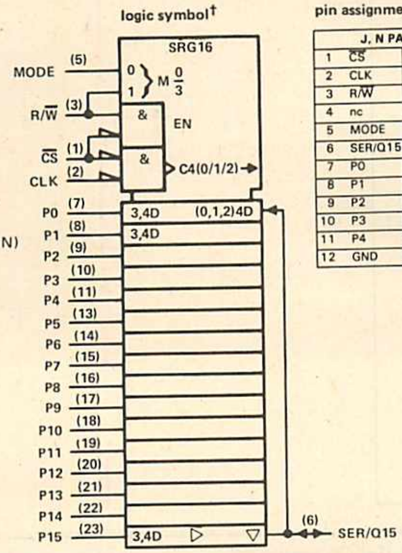
- Performs parallel to serial conversion
- Three-state outputs

typical performance

TYPE	SHIFT FREQ	TOTAL POWER
'LS674	20 MHz	125 mW

SN54LS674 (J,FH) SN74LS674 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{CS}$	13	P5
2	CLK	14	P6
3	R/$\overline{W}$	15	P7
4	nc	16	P8
5	MODE	17	P9
6	SER/Q15	18	P10
7	P0	19	P11
8	P1	20	P12
9	P2	21	P13
10	P3	22	P14
11	P4	23	P15
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{CS}$	16	P5
3	CLK	17	P6
4	R/$\overline{W}$	18	P7
5	nc	19	P8
6	MODE	20	P9
7	SER/Q15	21	P10
8	nc	22	nc
9	P0	23	P11
10	P1	24	P12
11	P2	25	P13
12	P3	26	P14
13	P4	27	P15
14	GND	28	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

677, 678

ADDRESS COMPARATORS

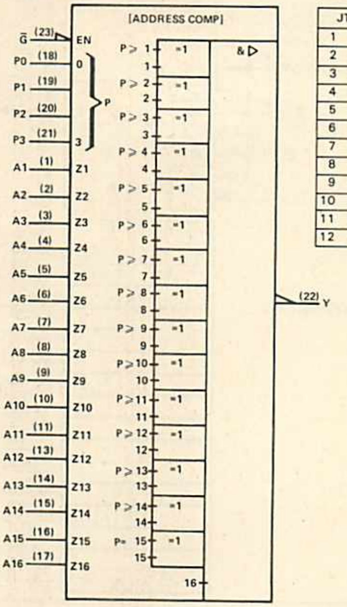
- 'ALS677 is a 16-bit to 4-bit comparator with enable
- 'ALS678 is a 16-bit to 4-bit comparator with latch

typical performance

TYPE	DELAY	POWER
'ALS677		
'ALS678		

SN54ALS677 (JT, FH) SN74ALS677 (NT, FN)
SN54ALS678 (JT, FH) SN74ALS678 (NT, FN)

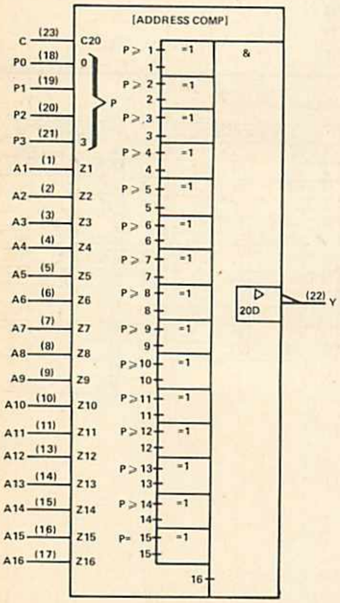
logic symbol, 'ALS677†



pin assignments, 'ALS677

JT, NT PACKAGES				FH, FN PACKAGES			
1	A1	13	A12	1	nc	15	nc
2	A2	14	A13	2	A1	16	A12
3	A3	15	A14	3	A2	17	A13
4	A4	16	A15	4	A3	18	A14
5	A5	17	A16	5	A4	19	A15
6	A6	18	P0	6	A5	20	A16
7	A7	19	P1	7	A6	21	P0
8	A8	20	P2	8	nc	22	nc
9	A9	21	P3	9	A7	23	P1
10	A10	22	Y	10	A8	24	P2
11	A11	23	$\overline{G}$	11	A9	25	P3
12	GND	24	V_{CC}	12	A10	26	Y
				13	A11	27	$\overline{G}$
				14	GND	28	V_{CC}

logic symbol, 'ALS678†



pin assignments, 'ALS678

JT, NT PACKAGES				FH, FN PACKAGES			
1	A1	13	A12	1	nc	15	nc
2	A2	14	A13	2	A1	16	A12
3	A3	15	A14	3	A2	17	A13
4	A4	16	A15	4	A3	18	A14
5	A5	17	A16	5	A4	19	A15
6	A6	18	P0	6	A5	20	A16
7	A7	19	P1	7	A6	21	P0
8	A8	20	P2	8	nc	22	nc
9	A9	21	P3	9	A7	23	P1
10	A10	22	Y	10	A8	24	P2
11	A11	23	C	11	A9	25	P3
12	GND	24	V_{CC}	12	A10	26	Y
				13	A11	27	C
				14	GND	28	V_{CC}

†Pin numbers shown on logic symbols are for JT and NT packages only.

nc — no internal connection.

679, 680

ADDRESS COMPARATORS

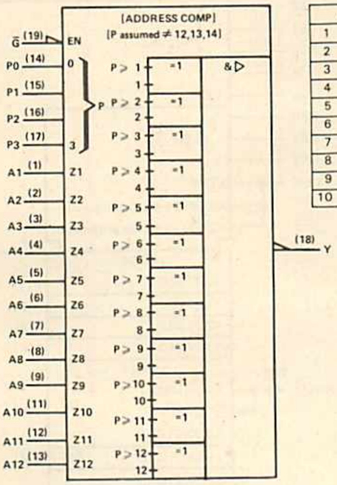
- 'ALS679 is a 12-bit to 4-bit comparator with enable
- 'ALS680 is a 12-bit to 4-bit comparator with latch

typical performance

TYPE	DELAY	POWER
'ALS679		
'ALS680		

SN54ALS679 (J,FH) SN74ALS679 (N,FN)
SN54ALS680 (J,FH) SN74ALS680 (N,FN)

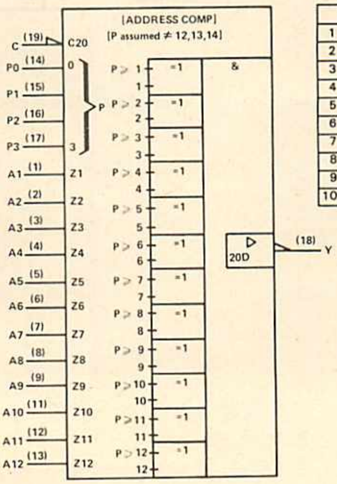
logic symbol, 'ALS679†



pin assignments, 'ALS679

J, N PACKAGES				FH, FN PACKAGES			
1	A1	11	A10	1	A1	11	A10
2	A2	12	A11	2	A2	12	A11
3	A3	13	A12	3	A3	13	A12
4	A4	14	P0	4	A4	14	P0
5	A5	15	P1	5	A5	15	P1
6	A6	16	P2	6	A6	16	P2
7	A7	17	P3	7	A7	17	P3
8	A8	18	Y	8	A8	18	Y
9	A9	19	$\overline{G}$	9	A9	19	$\overline{G}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol, 'ALS680†



pin assignments, 'ALS680

J, N PACKAGES				FH, FN PACKAGES			
1	A1	11	A10	1	A1	11	A10
2	A2	12	A11	2	A2	12	A11
3	A3	13	A12	3	A3	13	A12
4	A4	14	P0	4	A4	14	P0
5	A5	15	P1	5	A5	15	P1
6	A6	16	P2	6	A6	16	P2
7	A7	17	P3	7	A7	17	P3
8	A8	18	Y	8	A8	18	Y
9	A9	19	C	9	A9	19	C
10	GND	20	V_{CC}	10	GND	20	V_{CC}

---

†Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

681

4-BIT PARALLEL BINARY ACCUMULATORS

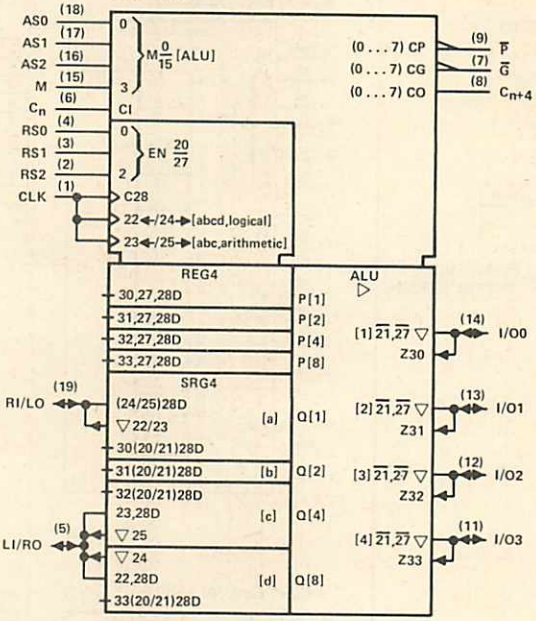
- Contains two synchronous registers
- B register frequency = 20 MHz
- Arithmetic operations include B minus A and A minus B
- Bus-driving I/O ports

typical performance

TYPE	LOAD TIME	ACC TIME
'LS681	75 ns	50 ns

SN54LS681 (J,FH)
SN74LS681 (J,N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	CLK	11	I/O3
2	RS2	12	I/O2
3	RS1	13	I/O1
4	RS0	14	I/O0
5	LI/RO	15	M
6	C_n	16	AS2
7	$\overline{G}$	17	AS1
8	C_{n+4}	18	AS0
9	$\overline{P}$	19	RI/LO
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	CLK	11	I/O3
2	RS2	12	I/O2
3	RS1	13	I/O1
4	RS0	14	I/O0
5	LI/RO	15	M
6	C_n	16	AS2
7	$\overline{G}$	17	AS1
8	C_{n+4}	18	AS0
9	$\overline{P}$	19	RI/LO
10	GND	20	V_{CC}

---

†Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

682, 683, 684, 685

8-BIT IDENTITY COMPARATORS

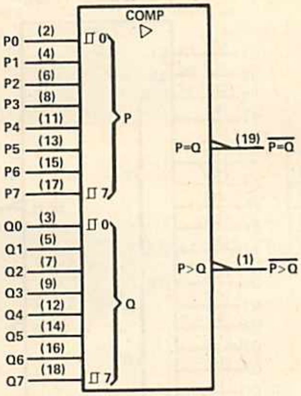
- *Compares two 8-bit words*
- 'LS682 and 'LS683 includes 20-kilohm pull-up resistor on Q inputs

typical performance

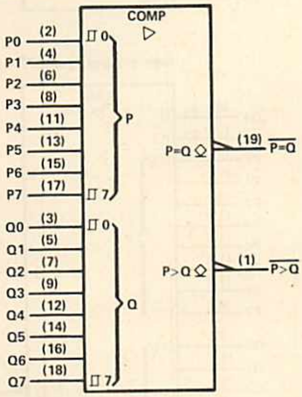
TYPE	COMPARE TIME	TYPE OUTPUT	TOTAL POWER
'LS682	14 ns	Totem Pole	210 mW
'LS683	24 ns	O-C	210 mW
'LS684	16 ns	Totem Pole	200 mW
'LS685	24 ns	O-C	200 mW

SN54LS682 (J,FH)	SN74LS682 (J,N,FN)
SN54LS683 (J,FH)	SN74LS683 (J,N,FN)
SN54LS684 (J,FH)	SN74LS684 (J,N,FN)
SN54LS685 (J,FH)	SN74LS685 (J,N,FN)

logic symbol, 'LS682, 'LS684 †



logic symbol, 'LS683, 'LS685†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{P>Q}$	11	P4	1	$\overline{P>Q}$	11	P4
2	P0	12	Q4	2	P0	12	Q4
3	Q0	13	P5	3	Q0	13	P5
4	P1	14	Q5	4	P1	14	Q5
5	Q1	15	P6	5	Q1	15	P6
6	P2	16	Q6	6	P2	16	Q6
7	Q2	17	P7	7	Q2	17	P7
8	P3	18	Q7	8	P3	18	Q7
9	Q3	19	$\overline{P=Q}$	9	Q3	19	$\overline{P=Q}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

686, 687

8-BIT IDENTITY COMPARATORS

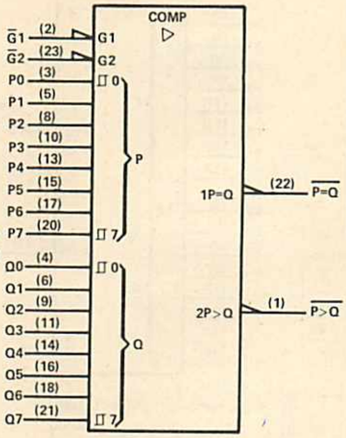
- Compares two 8-bit words

typical performance

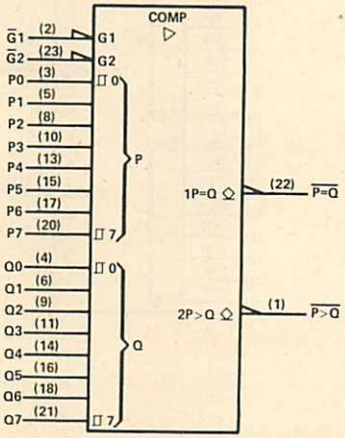
TYPE	COMPARE TIME	TYPE OUTPUT	TOTAL POWER
'LS686	17 ns	Totem-Pole	220 mW
'LS687	22 ns	O-C	220 mW

SN54LS686 (JT,FH) SN74LS686 (JT,NT,FN)
SN54LS687 (JT,FH) SN74LS687 (JT,NT,FN)

logic symbol, 'LS686†



logic symbol, 'LS687†



pin assignments

JT, NT PACKAGES				FH, FN PACKAGES			
1	$\overline{P>Q}$	13	P4	1	nc	15	nc
2	$\bar{G}$1	14	Q4	2	$\overline{P>Q}$	16	P4
3	P0	15	P5	3	$\bar{G}$1	17	Q4
4	Q0	16	Q5	4	P0	18	P5
5	P1	17	P6	5	Q0	19	Q5
6	Q1	18	Q6	6	P1	20	P6
7	nc	19	nc	7	Q1	21	Q6
8	P2	20	P7	8	nc	22	nc
9	Q2	21	Q7	9	nc	23	nc
10	P3	22	$\overline{P=Q}$	10	P2	24	P7
11	Q3	23	$\bar{G}$2	11	Q2	25	Q7
12	GND	24	V_{CC}	12	P3	26	$\overline{P=Q}$
				13	Q3	27	$\bar{G}$2
				14	GND	28	V_{CC}

---

†Pin numbers shown on logic symbols are for JT and NT packages only.
nc — no internal connection.

688, 689

8-BIT IDENTITY COMPARATORS

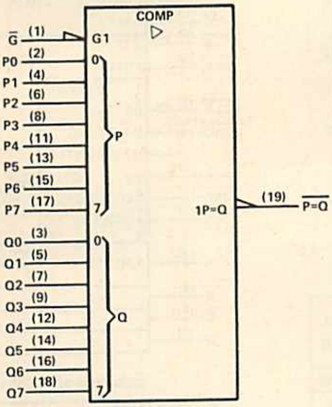
- Compares two 8-bit words

typical performance

TYPE	COMPARE TIME	TYPE OUTPUT	TOTAL POWER
'ALS688	9.5 ns	Totem-Pole	37.5 mW
'ALS689	15..5 ns	O-C	37.5 mW
'LS688	14.5 ns	Totem-Pole	200 mW
'LS689	23 ns	O-C	200 mW

SN54ALS688 (J,FH)	SN74ALS688 (J,FN)
SN54ALS689 (J,FH)	SN74ALS689 (N,FN)
SN54LS688 (J,FH)	SN74LS688 (J,N,FN)
SN54LS689 (J,FH)	SN74LS689 (J,N,FN)

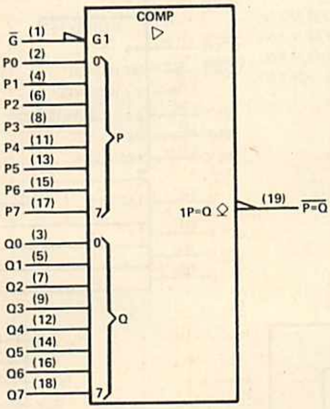
logic symbol, 'ALS688, 'LS688†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$	11	P4	1	$\overline{G}$	11	P4
2	P0	12	Q4	2	P0	12	Q4
3	Q0	13	P5	3	Q0	13	P5
4	P1	14	Q5	4	P1	14	Q5
5	Q1	15	P6	5	Q1	15	P6
6	P2	16	Q6	6	P2	16	Q6
7	Q2	17	P7	7	Q2	17	P7
8	P3	18	Q7	8	P3	18	Q7
9	Q3	19	$\overline{P=Q}$	9	Q3	19	$\overline{P=Q}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol, 'ALS689, 'LS689†



† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

690, 691
692, 693

SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS

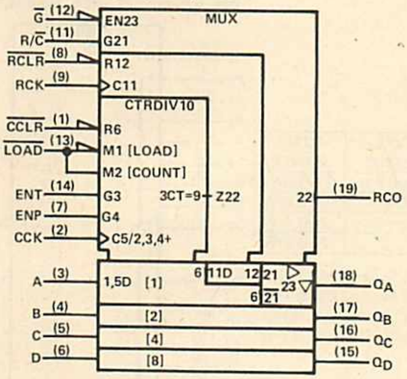
- Multiplexed three-state outputs
- 4-bit counters/registers
- 'LS690, 'LS692: Decade counters
- 'LS691, 'LS693: Binary counters

typical performance

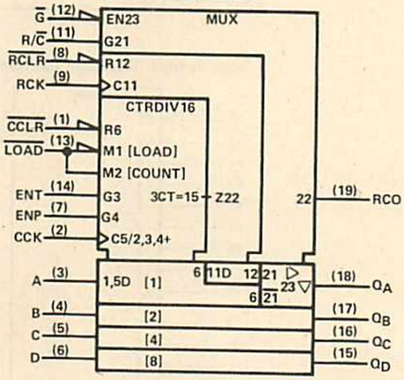
TYPE	CLEAR	MAX CLOCK FREQ	TOTAL POWER
'LS690	Direct	20 MHz	237 mW
'LS691	Direct	20 MHz	237 mW
'LS692	Sync-L	20 MHz	237 mW
'LS693	Sync-L	20 MHz	237 mW

SN54LS690 (J,FH)	SN74LS690 (J,N,FN)
SN54LS691 (J,FH)	SN74LS691 (J,N,FN)
SN54LS692 (J,FH)	SN74LS692 (J,N,FN)
SN54LS693 (J,FH)	SN74LS693 (J,N,FN)

logic symbol, 'LS690†



logic symbol, 'LS691†

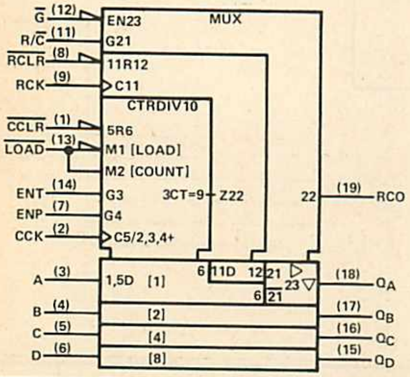


pin assignments

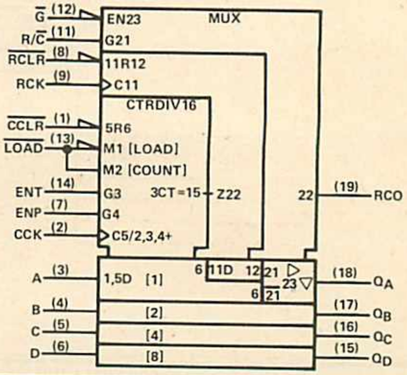
J, N PACKAGES			
1	CCLR	11	R/C
2	CCK	12	G
3	A	13	LOAD
4	B	14	ENT
5	C	15	Q_D
6	D	16	Q_C
7	ENP	17	Q_B
8	RCLR	18	Q_A
9	RCK	19	RCO
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	CCLR	11	R/C
2	CCK	12	G
3	A	13	LOAD
4	B	14	ENT
5	C	15	Q_D
6	D	16	Q_C
7	ENP	17	Q_B
8	RCLR	18	Q_A
9	RCK	19	RCO
10	GND	20	V_{CC}

logic symbol, 'LS692†



logic symbol, 'LS693†



† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

696, 697, 698, 699

SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS, MULTIPLEXED THREE-STATE OUTPUTS

- 4-bit counters/registers
- 'LS696, 'LS698: Decade counters
- 'LS697, 'LS699: Binary counters

typical performance

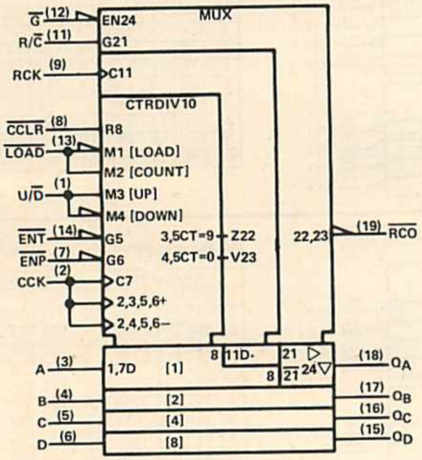
TYPE	MAX CLOCK FREQ	CLEAR	TOTAL POWER
'LS696	20 MHz	Async-L	237 mW
'LS697	20 MHz	Async-L	237 mW
'LS698	20 MHz	Sync-L	237 mW
'LS699	20 MHz	Sync-L	237 mW

SN54LS696 (J,FH)	SN74LS696 (J,N,FN)
SN54LS697 (J,FH)	SN74LS697 (J,N,FN)
SN54LS698 (J,FH)	SN74LS698 (J,N,FN)
SN54LS699 (J,FH)	SN74LS699 (J,N,FN)

pin assignments

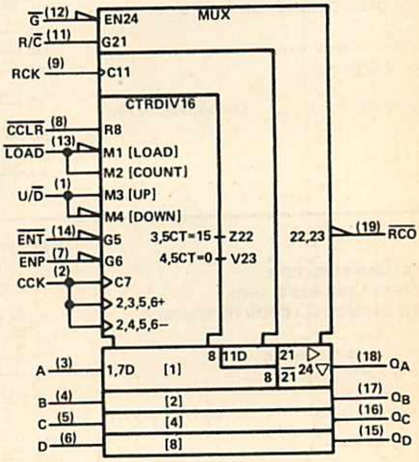
J, N PACKAGES				FH, FN PACKAGES			
1	U/$\overline{\text{D}}$	11	R/$\overline{\text{C}}$	1	U/D	11	R/$\overline{\text{C}}$
2	CCK	12	$\overline{\text{G}}$	2	CCK	12	$\overline{\text{G}}$
3	A	13	$\overline{\text{LOAD}}$	3	A	13	$\overline{\text{LOAD}}$
4	B	14	$\overline{\text{ENT}}$	4	B	14	$\overline{\text{ENT}}$
5	C	15	Q_D	5	C	15	Q_D
6	D	16	Q_C	6	D	16	Q_C
7	$\overline{\text{ENP}}$	17	Q_B	7	$\overline{\text{ENP}}$	17	Q_B
8	$\overline{\text{CCLR}}$	18	Q_A	8	$\overline{\text{CCLR}}$	18	Q_A
9	RCK	19	$\overline{\text{RCO}}$	9	RCK	19	$\overline{\text{RCO}}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol, 'LS696†



$\overline{\text{G}}$ (12)
R/$\overline{\text{C}}$ (11)
RCK (9)
$\overline{\text{CCLR}}$ (8)
$\overline{\text{LOAD}}$ (13)
U/$\overline{\text{D}}$ (1)
$\overline{\text{ENT}}$ (14)
$\overline{\text{ENP}}$ (7)
CCK (2)
EN24
MUX
G21
C11
CTRDIV10
R8
M1 [LOAD]
M2 [COUNT]
M3 [UP]
M4 [DOWN]
G5
G6
C7
2,3,5,6+
2,4,5,6−
3,5CT=9
4,5CT=0
Z22
V23
22,23
(19) $\overline{\text{RCO}}$
8 11D
21
8 21 24
A (3) 1,7D [1]
B (4) [2]
C (5) [4]
D (6) [8]
(18) Q_A
(17) Q_B
(16) Q_C
(15) Q_D

logic symbol, 'LS697†



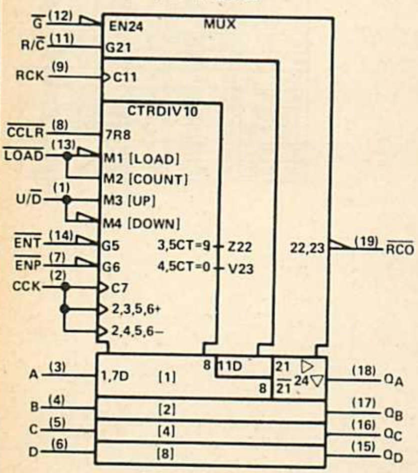
$\overline{\text{G}}$ (12)
R/$\overline{\text{C}}$ (11)
RCK (9)
$\overline{\text{CCLR}}$ (8)
$\overline{\text{LOAD}}$ (13)
U/$\overline{\text{D}}$ (1)
$\overline{\text{ENT}}$ (14)
$\overline{\text{ENP}}$ (7)
CCK (2)
EN24
MUX
G21
C11
CTRDIV16
R8
M1 [LOAD]
M2 [COUNT]
M3 [UP]
M4 [DOWN]
G5
G6
C7
2,3,5,6+
2,4,5,6−
3,5CT=15
4,5CT=0
Z22
V23
22,23
(19) $\overline{\text{RCO}}$
8 11D
21
8 21 24
A (3) 1,7D [1]
B (4) [2]
C (5) [4]
D (6) [8]
(18) Q_A
(17) Q_B
(16) Q_C
(15) Q_D

† Pin numbers shown on logic symbols are for J and N packages only.

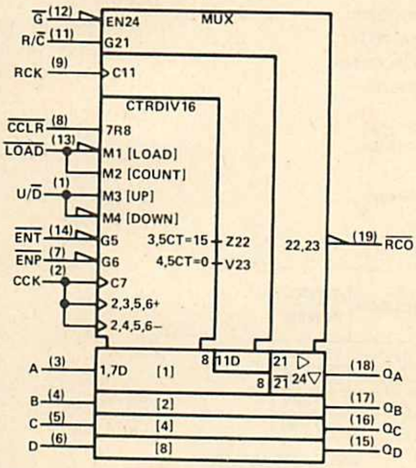
nc — no internal connection.

696, 697, 698, 699 continued

logic symbol, 'LS698†



logic symbol, 'LS699†



pin assignments

J, N PACKAGES			
1	U/$\overline{D}$	11	R/$\overline{C}$
2	CCK	12	$\overline{G}$
3	A	13	$\overline{LOAD}$
4	B	14	$\overline{ENT}$
5	C	15	Q_D
6	D	16	Q_C
7	$\overline{ENP}$	17	Q_B
8	$\overline{CCLR}$	18	Q_A
9	RCK	19	$\overline{RCO}$
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	U/$\overline{D}$	11	R/$\overline{C}$
2	CCK	12	$\overline{G}$
3	A	13	$\overline{LOAD}$
4	B	14	$\overline{ENT}$
5	C	15	Q_D
6	D	16	Q_C
7	$\overline{ENP}$	17	Q_B
8	$\overline{CCLR}$	18	Q_A
9	RCK	19	$\overline{RCO}$
10	GND	20	V_{CC}

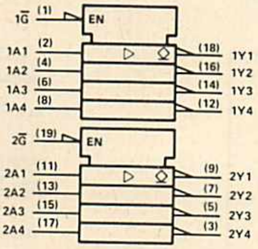
756

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS (WITH OPEN-COLLECTOR OUTPUTS)

- Open collector version of 'AS240

SN54AS756 (J,FH) SN74AS756 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1$\overline{G}$	11	2A1	1	1$\overline{G}$	11	2A1
2	1A1	12	1Y4	2	1A1	12	1Y4
3	2Y4	13	2A2	3	2Y4	13	2A2
4	1A2	14	1Y3	4	1A2	14	1Y3
5	2Y3	15	2A3	5	2Y3	15	2A3
6	1A3	16	1Y2	6	1A3	16	1Y2
7	2Y2	17	2A4	7	2Y2	17	2A4
8	1A4	18	1Y1	8	1A4	18	1Y1
9	2Y1	19	2$\overline{G}$	9	2Y1	19	2$\overline{G}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

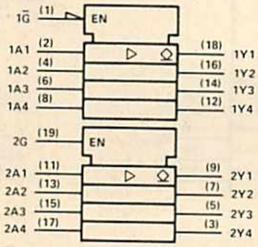
757

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS (WITH OPEN-COLLECTOR OUTPUTS)

- Open collector version of 'AS241

SN54AS757 (J,FH) SN74AS757 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1$\overline{G}$	11	2A1	1	1$\overline{G}$	11	2A1
2	1A1	12	1Y4	2	1A1	12	1Y4
3	2Y4	13	2A2	3	2Y4	13	2A2
4	1A2	14	1Y3	4	1A2	14	1Y3
5	2Y3	15	2A3	5	2Y3	15	2A3
6	1A3	16	1Y2	6	1A3	16	1Y2
7	2Y2	17	2A4	7	2Y2	17	2A4
8	1A4	18	1Y1	8	1A4	18	1Y1
9	2Y1	19	2G	9	2Y1	19	2G
10	GND	20	V_{CC}	10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

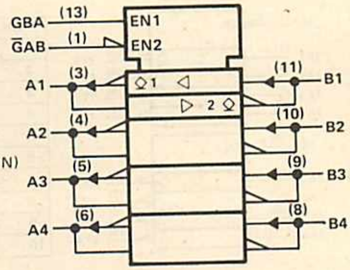
758

QUADRUPLE BUS TRANSCEIVERS (WITH OPEN-COLLECTOR OUTPUTS)

- Open-collector version of 'AS242

SN54AS758 (J,FH) SN74AS758 (N,FN)

logic symbol †



pin assignments

J,N PACKAGES			
1	$\overline{GAB}$	8	B4
2	nc	9	B3
3	A1	10	B2
4	A2	11	B1
5	A3	12	nc
6	A4	13	GBA
7	GND	14	V_{CC}

FH,FN PACKAGES			
1	nc	11	nc
2	$\overline{GAB}$	12	B4
3	nc	13	B3
4	A1	14	B2
5	nc	15	nc
6	A2	16	B1
7	nc	17	nc
8	A3	18	nc
9	A4	19	GBA
10	GND	20	V_{CC}

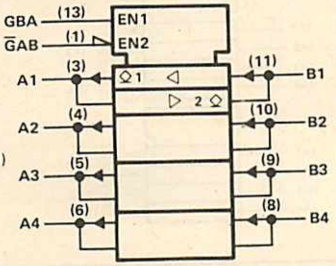
759

QUADRUPLE BUS TRANSCEIVERS (WITH OPEN-COLLECTOR OUTPUTS)

- Open-collector version of 'AS243

SN54AS759 (J,FH) SN74AS759 (N,FN)

logic symbol †



pin assignments

J,N PACKAGES			
1	$\overline{GAB}$	8	B4
2	nc	9	B3
3	A1	10	B2
4	A2	11	B1
5	A3	12	nc
6	A4	13	GBA
7	GND	14	V_{CC}

FH,FN PACKAGES			
1	nc	11	nc
2	$\overline{GAB}$	12	B4
3	nc	13	B3
4	A1	14	B2
5	nc	15	nc
6	A2	16	B1
7	nc	17	nc
8	A3	18	nc
9	A4	19	GBA
10	GND	20	V_{CC}

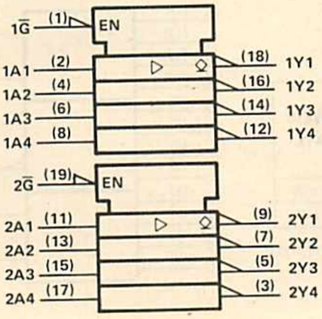
760

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS (WITH OPEN-COLLECTOR OUTPUTS)

- Open-collector version of 'AS244

SN54AS760 (J,FH) SN74AS760 (N,FN)

logic symbol †



pin assignments

J,N PACKAGES			
1	$1\overline{G}$	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	$2\overline{G}$
10	GND	20	V_{CC}

FH,FN PACKAGES			
1	$1\overline{G}$	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	$2\overline{G}$
10	GND	20	V_{CC}

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

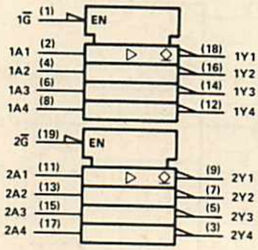
762, 763

OCTAL BUFFERS AND LINE DRIVERS (OPEN-COLLECTOR OUTPUTS)

- 'AS762 has true and complementary outputs
- 'AS763 has complementary G and $\overline{G}$ inputs
- 'AS762 is open-collector version of 'AS230
- 'AS763 is open-collector version of 'AS231

SN54AS762 (J,FH) SN74AS762 (N,FN)
SN54AS763 (J,FH) SN74AS763 (N,FN)

logic symbol 'AS762†



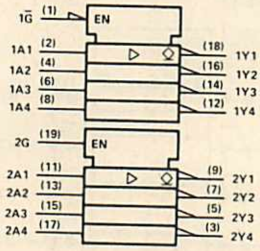
pin assignments

J,N PACKAGES			
1	$1\overline{G}$	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	$2\overline{G}$*
10	GND	20	V_{CC}

FH,FN PACKAGES			
1	$1\overline{G}$	11	2A1
2	1A1	12	1Y4
3	2Y4	13	2A2
4	1A2	14	1Y3
5	2Y3	15	2A3
6	1A3	16	1Y2
7	2Y2	17	2A4
8	1A4	18	1Y1
9	2Y1	19	$2\overline{G}$*
10	GND	20	V_{CC}

* 2G on 'AS763

logic symbol 'AS763



800

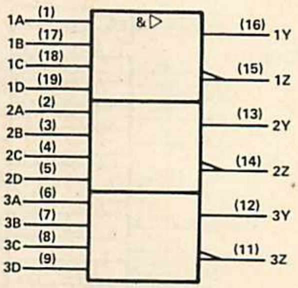
TRIPLE 4-INPUT AND/NAND DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	POWER/ GATE
SN54AS800	40 mA	−40 mA	25 mW
SN74AS800	48 mA	−48 mA	25 mW

SN54AS800 (J,FH) SN74AS800 (N,FN)

logic symbol†



positive logic: Y = ABCD
$Z = \overline{ABCD}$

pin assignments

J. N PACKAGES			
1	1A	11	3Z
2	2A	12	3Y
3	2B	13	2Y
4	2C	14	2Z
5	2D	15	1Z
6	3A	16	1Y
7	3B	17	1B
8	3C	18	1C
9	3D	19	1D
10	GND	20	V_{CC}

FH. FN PACKAGES			
1	1A	11	3Z
2	2A	12	3Y
3	2B	13	2Y
4	2C	14	2Z
5	2D	15	1Z
6	3A	16	1Y
7	3B	17	1B
8	3C	18	1C
9	3D	19	1D
10	GND	20	V_{CC}

802

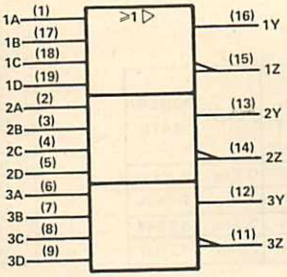
TRIPLE 4-INPUT OR/NOR LINE DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	POWER/ GATE
SN54AS802	40 mA	−40 mA	25 mW
SN74AS802	48 mA	−48 mA	25 mW

SN54AS802 (J,FH) SN74AS802 (N,FN)

logic symbol†



positive logic: $Y = A+B+C+D$

$Z = \overline{A+B+C+D}$

pin assignments

J, N PACKAGES			
1	1A	11	3Z
2	2A	12	3Y
3	2B	13	2Y
4	2C	14	2Z
5	2D	15	1Z
6	3A	16	1Y
7	3B	17	1B
8	3C	18	1C
9	3D	19	1D
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1A	11	3Z
2	2A	12	3Y
3	2B	13	2Y
4	2C	14	2Z
5	2D	15	1Z
6	3A	16	1Y
7	3B	17	1B
8	3C	18	1C
9	3D	19	1D
10	GND	20	V_{CC}

804

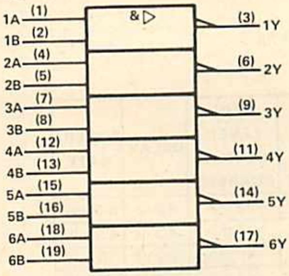
HEX 2-INPUT NAND DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/ GATE
SN54ALS804	12 mA	−12 mA	3 ns	3.4 mW
SN74ALS804	24 mA	−15 mA	3 ns	3.4 mW
SN54AS804A	40 mA	−40 mA	2.7 ns	9 mW
SN74AS804A	48 mA	−48 mA	2.7 ns	9 mW

SN54ALS804 (J,FH) SN74ALS804 (N,FN)
SN54AS804A (J,FH) SN74AS804A (N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

805

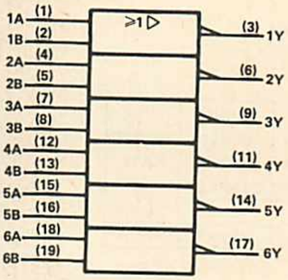
HEX 2-INPUT NOR DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/ GATE
SN54ALS805	12 mA	−12 mA	3.5 ns	4.2 mw
SN74ALS805	24 mA	−15 mA	3.5 ns	4.2 mW
SN54AS805A	40 mA	−40 mA	2.7 ns	12 mW
SN74AS805A	48 mA	−48 mA	2.7 ns	12 mW

SN54ALS805 (J,FH) SN74ALS805 (N,FN)
SN54AS805A (J,FH) SN74AS805A (N,FN)

logic symbol†



positive logic: $Y = \overline{A+B}$

pin assignments

J, N PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

808

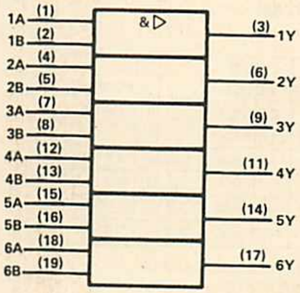
HEX 2-INPUT AND DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/ GATE
SN54ALS808	12 mA	−12 mA	4.3 ns	4.5 mW
SN74ALS808	24 mA	−15 mA	4.3 ns	4.5 mW
SN54AS808A	40 mA	−40 mA	3.2 ns	13 mW
SN74AS808A	48 mA	−48 mA	3.2 ns	13 mW

SN54ALS808 (J,FH) SN74ALS808 (N,FN)
SN54AS808A (J,FH) SN74AS808A (N,FN)

logic symbol†



positive logic: $Y = AB$

pin assignments

J, N PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

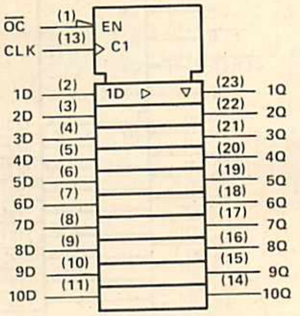
821

10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Non-inverting outputs

SN54AS821 (JT, FH) SN74AS821 (NT, FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	$\overline{OC}$	13	CLK
2	1D	14	10Q
3	2D	15	9Q
4	3D	16	8Q
5	4D	17	7Q
6	5D	18	6Q
7	6D	19	5Q
8	7D	20	4Q
9	8D	21	3Q
10	9D	22	2Q
11	10D	23	1Q
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{OC}$	16	CLK
3	1D	17	10Q
4	2D	18	9Q
5	3D	19	8Q
6	4D	20	7Q
7	5D	21	6Q
8	nc	22	nc
9	6D	23	5Q
10	7D	24	4Q
11	8D	25	3Q
12	9D	26	2Q
13	10D	27	1Q
14	GND	28	V_{CC}

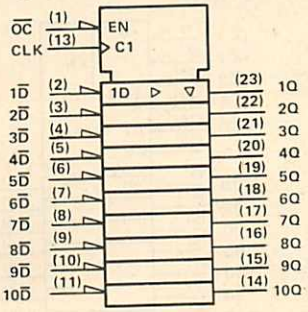
822

10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Inverting outputs

SN54AS822 (JT, FH) SN74AS822 (NT, FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	$\overline{OC}$	13	CLK
2	$1\overline{D}$	14	10Q
3	$2\overline{D}$	15	9Q
4	$3\overline{D}$	16	8Q
5	$4\overline{D}$	17	7Q
6	$5\overline{D}$	18	6Q
7	$6\overline{D}$	19	5Q
8	$7\overline{D}$	20	4Q
9	$8\overline{D}$	21	3Q
10	$9\overline{D}$	22	2Q
11	$10\overline{D}$	23	1Q
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{OC}$	16	CLK
3	$1\overline{D}$	17	10Q
4	$2\overline{D}$	18	9Q
5	$3\overline{D}$	19	8Q
6	$4\overline{D}$	20	7Q
7	$5\overline{D}$	21	6Q
8	nc	22	nc
9	$6\overline{D}$	23	5Q
10	$7\overline{D}$	24	4Q
11	$8\overline{D}$	25	3Q
12	$9\overline{D}$	26	2Q
13	$10\overline{D}$	27	1Q
14	GND	28	V_{CC}

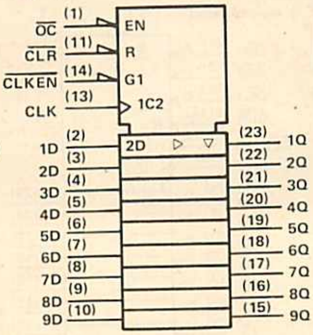
823

9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Non-inverting outputs

SN54AS823 (JT, FH) SN74AS823 (NT, FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	$\overline{OC}$	13	CLK
2	1D	14	$\overline{CLKEN}$
3	2D	15	9Q
4	3D	16	8Q
5	4D	17	7Q
6	5D	18	6Q
7	6D	19	5Q
8	7D	20	4Q
9	8D	21	3Q
10	9D	22	2Q
11	$\overline{CLR}$	23	1Q
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{OC}$	16	CLK
3	1D	17	$\overline{CLKEN}$
4	2D	18	9Q
5	3D	19	8Q
6	4D	20	7Q
7	5D	21	6Q
8	nc	22	nc
9	6D	23	5Q
10	7D	24	4Q
11	8D	25	3Q
12	9D	26	2Q
13	$\overline{CLR}$	27	1Q
14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for JT and NT packages only.

nc — no internal connection.

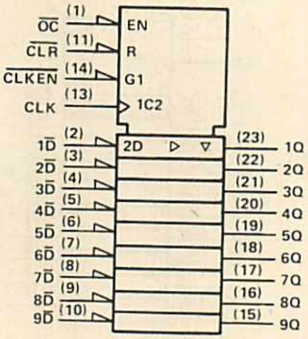
824

9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Inverting outputs

SN54AS824 (JT,FH)
SN74AS824 (NT,FN)

logic symbol†


$\overline{\mathrm{OC}}$ (1)
EN
$\overline{\mathrm{CLR}}$ (11)
R
$\overline{\mathrm{CLKEN}}$ (14)
G1
CLK (13)
1C2
$1\overline{\mathrm{D}}$ (2)
2D
(23) 1Q
$2\overline{\mathrm{D}}$ (3)
(22) 2Q
$3\overline{\mathrm{D}}$ (4)
(21) 3Q
$4\overline{\mathrm{D}}$ (5)
(20) 4Q
$5\overline{\mathrm{D}}$ (6)
(19) 5Q
$6\overline{\mathrm{D}}$ (7)
(18) 6Q
$7\overline{\mathrm{D}}$ (8)
(17) 7Q
$8\overline{\mathrm{D}}$ (9)
(16) 8Q
$9\overline{\mathrm{D}}$ (10)
(15) 9Q

pin assignments

JT, NT PACKAGES			
1	$\overline{\mathrm{OC}}$	13	CLK
2	$1\overline{\mathrm{D}}$	14	$\overline{\mathrm{CLKEN}}$
3	$2\overline{\mathrm{D}}$	15	9Q
4	$3\overline{\mathrm{D}}$	16	8Q
5	$4\overline{\mathrm{D}}$	17	7Q
6	$5\overline{\mathrm{D}}$	18	6Q
7	$6\overline{\mathrm{D}}$	19	5Q
8	$7\overline{\mathrm{D}}$	20	4Q
9	$8\overline{\mathrm{D}}$	21	3Q
10	$9\overline{\mathrm{D}}$	22	2Q
11	$\overline{\mathrm{CLR}}$	23	1Q
12	GND	24	$\mathrm{V_{CC}}$

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{\mathrm{OC}}$	16	CLK
3	$1\overline{\mathrm{D}}$	17	$\overline{\mathrm{CLKEN}}$
4	$2\overline{\mathrm{D}}$	18	9Q
5	$3\overline{\mathrm{D}}$	19	8Q
6	$4\overline{\mathrm{D}}$	20	7Q
7	$5\overline{\mathrm{D}}$	21	6Q
8	nc	22	nc
9	$6\overline{\mathrm{D}}$	23	5Q
10	$7\overline{\mathrm{D}}$	24	4Q
11	$8\overline{\mathrm{D}}$	25	3Q
12	$9\overline{\mathrm{D}}$	26	2Q
13	$\overline{\mathrm{CLR}}$	27	1Q
14	GND	28	$\mathrm{V_{CC}}$

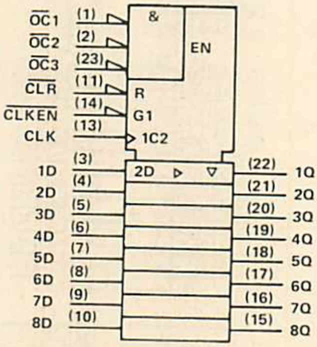
825

8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Non-inverting outputs

SN54AS825 (JT,FH)
SN74AS825 (NT,FN)

logic symbol†


$\overline{\mathrm{OC}}1$ (1)
$\overline{\mathrm{OC}}2$ (2)
$\overline{\mathrm{OC}}3$ (23)
&
EN
$\overline{\mathrm{CLR}}$ (11)
R
$\overline{\mathrm{CLKEN}}$ (14)
G1
CLK (13)
1C2
1D (3)
2D
(22) 1Q
2D (4)
(21) 2Q
3D (5)
(20) 3Q
4D (6)
(19) 4Q
5D (7)
(18) 5Q
6D (8)
(17) 6Q
7D (9)
(16) 7Q
8D (10)
(15) 8Q

pin assignments

JT, NT PACKAGES			
1	$\overline{\mathrm{OC1}}$	13	CLK
2	$\overline{\mathrm{OC2}}$	14	$\overline{\mathrm{CLKEN}}$
3	1D	15	8Q
4	2D	16	7Q
5	3D	17	6Q
6	4D	18	5Q
7	5D	19	4Q
8	6D	20	3Q
9	7D	21	2Q
10	8D	22	1Q
11	$\overline{\mathrm{CLR}}$	23	$\overline{\mathrm{OC3}}$
12	GND	24	$\mathrm{V_{CC}}$

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{\mathrm{OC1}}$	16	CLK
3	$\overline{\mathrm{OC2}}$	17	$\overline{\mathrm{CLKEN}}$
4	1D	18	8Q
5	2D	19	7Q
6	3D	20	6Q
7	4D	21	5Q
8	nc	22	nc
9	5D	23	4Q
10	6D	24	3Q
11	7D	25	2Q
12	8D	26	1Q
13	$\overline{\mathrm{CLR}}$	27	$\overline{\mathrm{OC3}}$
14	GND	28	$\mathrm{V_{CC}}$

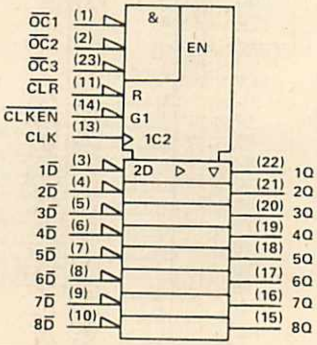
826

8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Inverting outputs

SN54AS825 (JT,FH)
SN74AS825 (NT,FN)

logic symbol†


$\overline{\mathrm{OC}}1$ (1)
$\overline{\mathrm{OC}}2$ (2)
$\overline{\mathrm{OC}}3$ (23)
&
EN
$\overline{\mathrm{CLR}}$ (11)
R
$\overline{\mathrm{CLKEN}}$ (14)
G1
CLK (13)
1C2
$1\overline{\mathrm{D}}$ (3)
2D
(22) 1Q
$2\overline{\mathrm{D}}$ (4)
(21) 2Q
$3\overline{\mathrm{D}}$ (5)
(20) 3Q
$4\overline{\mathrm{D}}$ (6)
(19) 4Q
$5\overline{\mathrm{D}}$ (7)
(18) 5Q
$6\overline{\mathrm{D}}$ (8)
(17) 6Q
$7\overline{\mathrm{D}}$ (9)
(16) 7Q
$8\overline{\mathrm{D}}$ (10)
(15) 8Q

pin assignments

JT, NT PACKAGES			
1	$\overline{\mathrm{OC1}}$	13	CLK
2	$\overline{\mathrm{OC2}}$	14	$\overline{\mathrm{CLKEN}}$
3	$1\overline{\mathrm{D}}$	15	8Q
4	$2\overline{\mathrm{D}}$	16	7Q
5	$3\overline{\mathrm{D}}$	17	6Q
6	$4\overline{\mathrm{D}}$	18	5Q
7	$5\overline{\mathrm{D}}$	19	4Q
8	$6\overline{\mathrm{D}}$	20	3Q
9	$7\overline{\mathrm{D}}$	21	2Q
10	$8\overline{\mathrm{D}}$	22	1Q
11	$\overline{\mathrm{CLR}}$	23	$\overline{\mathrm{OC3}}$
12	GND	24	$\mathrm{V_{CC}}$

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{\mathrm{OC1}}$	16	CLK
3	$\overline{\mathrm{OC2}}$	17	$\overline{\mathrm{CLKEN}}$
4	$1\overline{\mathrm{D}}$	18	8Q
5	$2\overline{\mathrm{D}}$	19	7Q
6	$3\overline{\mathrm{D}}$	20	6Q
7	$4\overline{\mathrm{D}}$	21	5Q
8	nc	22	nc
9	$5\overline{\mathrm{D}}$	23	4Q
10	$6\overline{\mathrm{D}}$	24	3Q
11	$7\overline{\mathrm{D}}$	25	2Q
12	$8\overline{\mathrm{D}}$	26	1Q
13	$\overline{\mathrm{CLR}}$	27	$\overline{\mathrm{OC3}}$
14	GND	28	$\mathrm{V_{CC}}$

† Pin numbers shown on logic symbols are for JT and NT packages only.
nc — no internal connection.

832

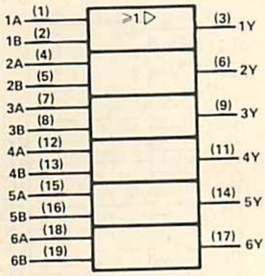
HEX 2-INPUT OR DRIVERS

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/ GATE
SN54ALS832	12 mA	– 12 mA	4 ns	5.3 mW
SN74ALS832	24 mA	– 15 mA	4 ns	5.3 mW
SN54AS832A	40 mA	– 40 mA	3 ns	17 mW
SN74AS832A	48 mA	– 48 mA	3 ns	17 mW

SN54ALS832 (J,FH)   SN74ALS832 (N,FN)
SN54AS832A (J,FH)   SN74AS832A (N,FN)

logic symbol†



positive logic: Y = A+B

pin assignments

FH,FN PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

J,N PACKAGES			
1	1A	11	4Y
2	1B	12	4A
3	1Y	13	4B
4	2A	14	5Y
5	2B	15	5A
6	2Y	16	5B
7	3A	17	6Y
8	3B	18	6A
9	3Y	19	6B
10	GND	20	V_{CC}

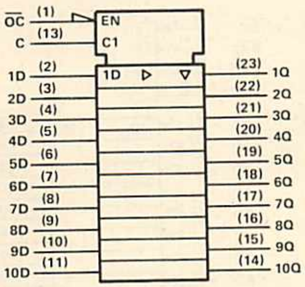
841

10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- High-speed parallel latches — noninverting transparent
-

SN54AS841 (JT, FH)   SN74AS841 (NT, FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	$\overline{OC}$	13	C
2	1D	14	10Q
3	2D	15	9Q
4	3D	16	8Q
5	4D	17	7Q
6	5D	18	6Q
7	6D	19	5Q
8	7D	20	4Q
9	8D	21	3Q
10	9D	22	2Q
11	10D	23	1Q
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{OC}$	16	C
3	1D	17	10Q
4	2D	18	9Q
5	3D	19	8Q
6	4D	20	7Q
7	5D	21	6Q
8	nc	22	nc
9	6D	23	5Q
10	7D	24	4Q
11	8D	25	3Q
12	9D	26	2Q
13	10D	27	1Q
14	GND	28	V_{CC}

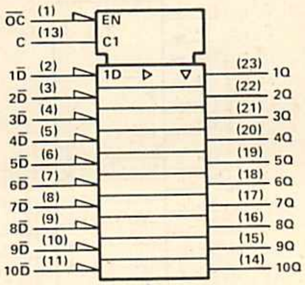
842

10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- High-speed parallel latches — inverting transparent

SN54AS842 (JT, FH)   SN74AS842 (NT, FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	$\overline{OC}$	13	C
2	$1\overline{D}$	14	10Q
3	$2\overline{D}$	15	9Q
4	$3\overline{D}$	16	8Q
5	$4\overline{D}$	17	7Q
6	$5\overline{D}$	18	6Q
7	$6\overline{D}$	19	5Q
8	$7\overline{D}$	20	4Q
9	$8\overline{D}$	21	3Q
10	$9\overline{D}$	22	2Q
11	$10\overline{D}$	23	1Q
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{OC}$	16	C
3	$1\overline{D}$	17	10Q
4	$2\overline{D}$	18	9Q
5	$3\overline{D}$	19	8Q
6	$4\overline{D}$	20	7Q
7	$5\overline{D}$	21	6Q
8	nc	22	nc
9	$6\overline{D}$	23	5Q
10	$7\overline{D}$	24	4Q
11	$8\overline{D}$	25	3Q
12	$9\overline{D}$	26	2Q
13	$10\overline{D}$	27	1Q
14	GND	28	V_{CC}

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† Pin numbers shown on logic symbols are for J, JT, N, NT packages only.
nc — no internal connection.

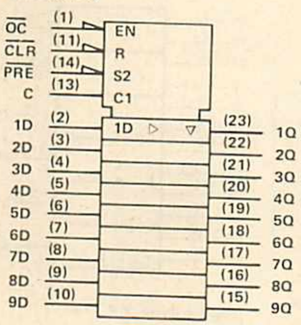
843

9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- High-speed parallel latches — noninverting transparent

SN54AS843 (JT, FH) SN74AS943 (NT, FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	$\overline{\text{OC}}$	13	C
2	1D	14	$\overline{\text{PRE}}$
3	2D	15	9Q
4	3D	16	8Q
5	4D	17	7Q
6	5D	18	6Q
7	6D	19	5Q
8	7D	20	4Q
9	8D	21	3Q
10	9D	22	2Q
11	$\overline{\text{CLR}}$	23	1Q
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{\text{OC}}$	16	C
3	1D	17	$\overline{\text{PRE}}$
4	2D	18	9Q
5	3D	19	8Q
6	4D	20	7Q
7	5D	21	6Q
8	nc	22	nc
9	6D	23	5Q
10	7D	24	4Q
11	8D	25	3Q
12	9D	26	2Q
13	$\overline{\text{CLR}}$	27	1Q
14	GND	28	V_{CC}

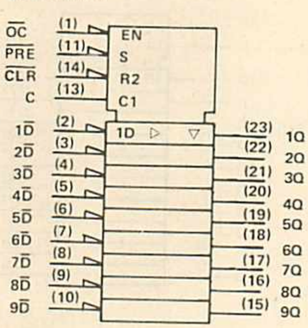
844

9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- High-speed parallel latches — inverting transparent

SN54AS844 (JT, FH) SN74AS844 (NT, FN)

logic symbol†


$\overline{\text{OC}}$ (1) EN
$\overline{\text{PRE}}$ (11) S
$\overline{\text{CLR}}$ (14) R2
C (13) C1
$1\overline{\text{D}}$ (2) 1D ▷ ▽ (23) 1Q
$2\overline{\text{D}}$ (3) (22) 2Q
$3\overline{\text{D}}$ (4) (21) 3Q
$4\overline{\text{D}}$ (5) (20) 4Q
$5\overline{\text{D}}$ (6) (19) 5Q
$6\overline{\text{D}}$ (7) (18) 6Q
$7\overline{\text{D}}$ (8) (17) 7Q
$8\overline{\text{D}}$ (9) (16) 8Q
$9\overline{\text{D}}$ (10) (15) 9Q

pin assignments

JT, NT PACKAGES			
1	$\overline{\text{OC}}$	13	C
2	$1\overline{\text{D}}$	14	$\overline{\text{CLR}}$
3	$2\overline{\text{D}}$	15	9Q
4	$3\overline{\text{D}}$	16	8Q
5	$4\overline{\text{D}}$	17	7Q
6	$5\overline{\text{D}}$	18	6Q
7	$6\overline{\text{D}}$	19	5Q
8	$7\overline{\text{D}}$	20	4Q
9	$8\overline{\text{D}}$	21	3Q
10	$9\overline{\text{D}}$	22	2Q
11	$\overline{\text{PRE}}$	23	1Q
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{\text{OC}}$	16	C
3	1D	17	$\overline{\text{CLR}}$
4	2D	18	9Q
5	3D	19	8Q
6	4D	20	7Q
7	5D	21	6Q
8	nc	22	nc
9	6D	23	5Q
10	7D	24	4Q
11	8D	25	3Q
12	9D	26	2Q
13	$\overline{\text{PRE}}$	27	1Q
14	GND	28	V_{CC}

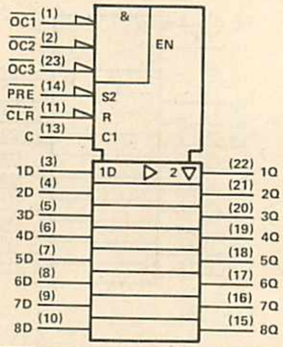
845

8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- High-speed parallel latches — noninverting transparent

SN54AS845 (JT, FH) SN74AS845 (NT, FN)

logic symbol†


$\overline{\text{OC1}}$ (1) &
$\overline{\text{OC2}}$ (2) EN
$\overline{\text{OC3}}$ (23)
$\overline{\text{PRE}}$ (14) S2
$\overline{\text{CLR}}$ (11) R
C (13) C1
1D (3) 1D ▷ 2▽ (22) 1Q
2D (4) (21) 2Q
3D (5) (20) 3Q
4D (6) (19) 4Q
5D (7) (18) 5Q
6D (8) (17) 6Q
7D (9) (16) 7Q
8D (10) (15) 8Q

pin assignments

JT, NT PACKAGES			
1	$\overline{\text{OC1}}$	13	C
2	$\overline{\text{OC2}}$	14	$\overline{\text{PRE}}$
3	1D	15	8Q
4	2D	16	7Q
5	3D	17	6Q
6	4D	18	5Q
7	5D	19	4Q
8	6D	20	3Q
9	7D	21	2Q
10	8D	22	1Q
11	$\overline{\text{CLR}}$	23	$\overline{\text{OC3}}$
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{\text{OC1}}$	16	C
3	$\overline{\text{OC2}}$	17	$\overline{\text{PRE}}$
4	1D	18	8Q
5	2D	19	7Q
6	3D	20	6Q
7	4D	21	5Q
8	nc	22	nc
9	5D	23	4Q
10	6D	24	3Q
11	7D	25	2Q
12	8D	26	1Q
13	$\overline{\text{CLR}}$	27	$\overline{\text{OC3}}$
14	GND	28	V_{CC}

† Pin numbers shown on logic symbols are for JT and NT packages only.
nc — no internal connection.

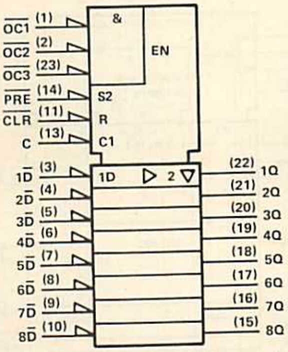
846

8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- High-speed parallel latches — inverting transparent

SN54AS846 (JT, FH) SN74AS846 (NT, FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	$\overline{\mathrm{OC}}1$	13	C
2	$\overline{\mathrm{OC}}2$	14	$\overline{\mathrm{CLR}}$
3	$1\overline{D}$	15	8Q
4	$2\overline{D}$	16	7Q
5	$3\overline{D}$	17	6Q
6	$4\overline{D}$	18	5Q
7	$5\overline{D}$	19	4Q
8	$6\overline{D}$	20	3Q
9	$7\overline{D}$	21	2Q
10	$8\overline{D}$	22	1Q
11	$\overline{\mathrm{PRE}}$	23	$\overline{\mathrm{OC}}3$
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{\mathrm{OC}}1$	16	C
3	$\overline{\mathrm{OC}}2$	17	$\overline{\mathrm{CLR}}$
4	1D	18	8Q
5	2D	19	7Q
6	3D	20	6Q
7	4D	21	5Q
8	nc	22	nc
9	5D	23	4Q
10	6D	24	3Q
11	7D	25	2Q
12	8D	26	1Q
13	$\overline{\mathrm{PRE}}$	27	$\overline{\mathrm{OC}}3$
14	GND	28	V_{CC}

850, 851

1 OF 16 DATA SELECTORS/MULTIPLEXERS

- Registered select lines (850)
- Latched select lines (851)
- 4 ns data to output
- 7 ns clock to output
- Three-state outputs controls for both outputs

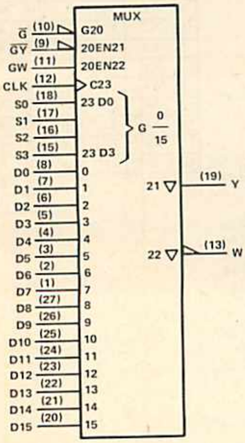
SN54AS850 (JD, FH) SN74AS850 (N, FN)
SN54AS851 (JD, FH) SN74AS851 (N, FN)

pin assignments

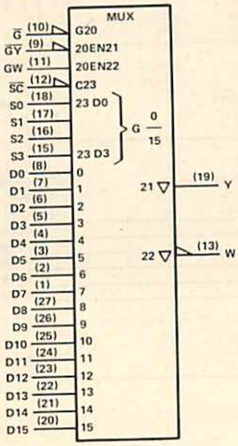
JD, N PACKAGES			
1	E7	15	D
2	E6	16	C
3	E5	17	B
4	E4	18	A
5	E3	19	Y
6	E2	20	E15
7	E1	21	E14
8	E0	22	E13
9	$\overline{G}Y/\overline{GY}$	23	E12
10	$\overline{G}/G$	24	E11
11	GW	25	E10
12	CK/GL	26	E9
13	$\overline{W}$	27	E8
14	GND	28	V_{CC}

FH, FN PACKAGES			
1	E7	15	D
2	E6	16	C
3	E5	17	B
4	E4	18	A
5	E3	19	Y
6	E2	20	E15
7	E1	21	E14
8	E0	22	E13
9	$\overline{G}Y/\overline{GY}$	23	E12
10	$\overline{G}/G$	24	E11
11	GW	25	E10
12	CK/GL	26	E9
13	$\overline{W}$	27	E8
14	GND	28	V_{CC}

logic symbol† 'AS850



logic symbol† 'AS851



† Pin numbers shown on logic symbols are for JD, JT, N, and NT packages only.
nc — no internal connection.

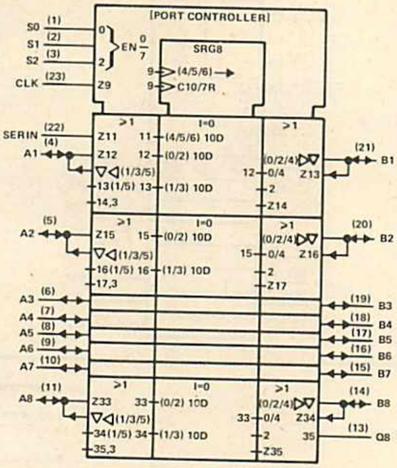
852

8-BIT UNIVERSAL TRANSCEIVER/PORT CONTROLLERS

- 8 selectable transceivert/port functions
- 3-state buffer-type outputs drive bus lines directly
- 24-pin 300-mil package

SN54AS852 (JT,FH)
SN74AS852 (NT,FN)

logic symbol†



pin assignments

JT,NT PACKAGES			
1	S0	13	Q8
2	S1	14	B8
3	S2	15	B7
4	A1	16	B6
5	A2	17	B5
6	A3	18	B4
7	A4	19	B3
8	A5	20	B2
9	A6	21	B1
10	A7	22	SERIN
11	A8	23	CLK
12	GND	24	V_{CC}

FH,FN PACKAGES			
1	nc	15	nc
2	S0	16	Q8
3	S1	17	B8
4	S2	18	B7
5	A1	19	B6
6	A2	20	B5
7	A3	21	B4
8	nc	22	nc
9	A4	23	B3
10	A5	24	B2
11	A6	25	B1
12	A7	26	SERIN
13	A8	27	CLK
14	GND	28	V_{CC}

For further information, contact the factory.

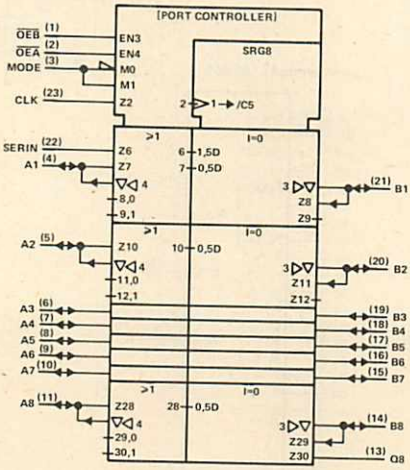
856

8-BIT UNIVERSAL TRANSCEIVER/PORT CONTROLLERS

- 8 selectable transceiver/port functions
- 3-state buffer-type outputs drive bus lines directly
- 24-pin 300-mil package

SN54AS856 (JT,FH)
SN74AS856 (NT,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	$\overline{\text{OEB}}$	13	Q8
2	$\overline{\text{OEA}}$	14	B8
3	MODE	15	B7
4	A1	16	B6
5	A2	17	B5
6	A3	18	B4
7	A4	19	B3
8	A5	20	B2
9	A6	21	B1
10	A7	22	SERIN
11	A8	23	CLK
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{\text{OEB}}$	16	Q8
3	$\overline{\text{OEA}}$	17	B8
4	MODE	18	B7
5	A1	19	B6
6	A2	20	B5
7	A3	21	B4
8	nc	22	nc
9	A4	23	B3
10	A5	24	B2
11	A6	25	B1
12	A7	26	SERIN
13	A8	27	CLK
14	GND	28	V_{CC}

For further information, contact the factory.

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† Pin numbers shown on logic symbols are for JT and NT packages only.
nc — no internal connection.

857

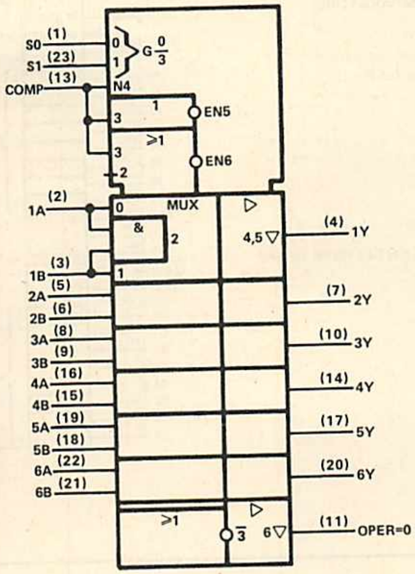
HEX 2-TO-1 UNIVERSAL MULTIPLEXER

- Three-state buffer-type outputs
- True or complementary data

SN54ALS857 (JT)
SN54AS857 (JT,FH)

SN74ALS857 (JT,NT)
SN74AS857 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	S0	13	COMP
2	1A	14	4Y
3	1B	15	4B
4	1Y	16	4A
5	2A	17	5Y
6	2B	18	5B
7	2Y	19	5A
8	3A	20	6Y
9	3B	21	6B
10	3Y	22	6A
11	OPER = 0	23	S1
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	S0	16	COMP
3	1A	17	4Y
4	1B	18	4B
5	1Y	19	4A
6	2A	20	5Y
7	2B	21	5B
8	nc	22	nc
9	2Y	23	5A
10	3A	24	6Y
11	3B	25	6B
12	3Y	26	6A
13	OPER = 0	27	S1
14	GND	28	V_{CC}

---

† Pin numbers shown on logic symbols are for J, JT, N, and NT packages only.

nc — no internal connection.

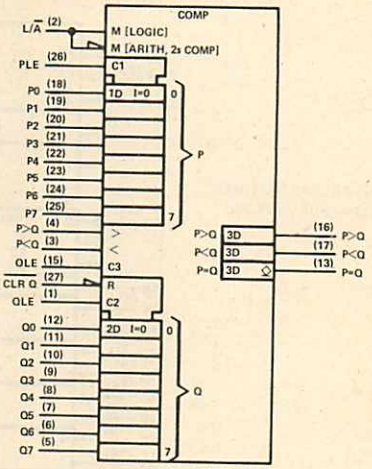
866

8-BIT MAGNITUDE COMPARATORS

- Fast compare to zero
- Arithmetic and logical comparison
- Open-collector output for P = Q

SN54AS866 (JD,FH)   SN74AS866 (N,FN)

logic symbol†



pin assignments

JD, N PACKAGES			
1	QLE	15	OLE
2	L/$\overline{\text{A}}$	16	P>Qout
3	P<Qin	17	P<Qout
4	P>Qin	18	P0
5	Q7	19	P1
6	Q6	20	P2
7	Q5	21	P3
8	Q4	22	P4
9	Q3	23	P5
10	Q2	24	P6
11	Q1	25	P7
12	Q0	26	PLE
13	P = Qout	27	$\overline{\text{CLRQ}}$
14	GND	28	V_{CC}

FH, FN PACKAGES			
1	QLE	15	OLE
2	L/$\overline{\text{A}}$	16	P>Qout
3	P<Qin	17	P<Qout
4	P>Qin	18	P0
5	Q7	19	P1
6	Q6	20	P2
7	Q5	21	P3
8	Q4	22	P4
9	Q3	23	P5
10	Q2	24	P6
11	Q1	25	P7
12	Q0	26	PLE
13	P = Qout	27	$\overline{\text{CLRQ}}$
14	GND	28	V_{CC}

867, 869

8-BIT SYNCHRONOUS BIDIRECTIONAL COUNTERS

- 'AS867 has asynchronous clear
- 'AS869 has synchronous clear
- Ripple carry output for N-bit cascading
- Fully programmable with synchronous counting and loading

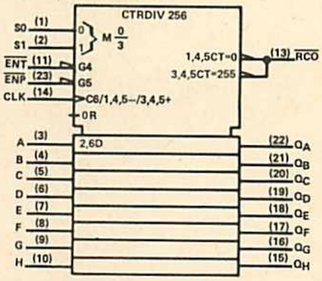
FUNCTION TABLE

S1	S0	FUNCTION
L	L	Clear
L	H	Count Down
H	L	Load
H	H	Count Up

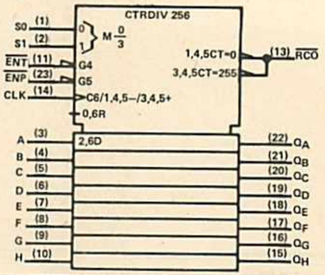
Supersedes table in *1981 Supplement to TTL Data Book*

SN54AS867 (JT,FH)   SN74AS867 (NT,FN)
SN54AS869 (JT,FH)   SN74AS869 (NT,FN)

logic symbol, 'AS867†



logic symbol, 'AS869†



pin assignments

JT, NT PACKAGES			
1	S0	13	$\overline{\text{RCO}}$
2	S1	14	CLK
3	A	15	Q_H
4	B	16	Q_G
5	C	17	Q_F
6	D	18	Q_E
7	E	19	Q_D
8	F	20	Q_C
9	G	21	Q_B
10	H	22	Q_A
11	$\overline{\text{ENT}}$	23	$\overline{\text{ENP}}$
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	S0	16	$\overline{\text{RCO}}$
3	S1	17	CLK
4	A	18	Q_H
5	B	19	Q_G
6	C	20	Q_F
7	D	21	Q_E
8	nc	22	nc
9	E	23	Q_D
10	F	24	Q_C
11	G	25	Q_B
12	H	26	Q_A
13	$\overline{\text{ENT}}$	27	$\overline{\text{ENP}}$
14	GND	28	V_{CC}

---

†Pin numbers shown on logic symbols are for JT and NT packages only.

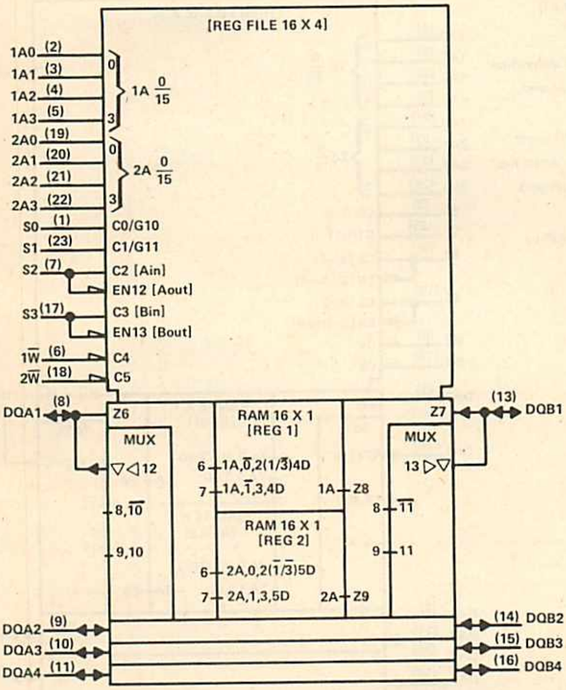
870

DUAL 16-BY-4 REGISTER FILES

- Each register file has individual write/enable controls and address lines
- Has two 4-bit data I/O ports
- 24-pin 300-mil package

SN54AS870 (JT,FH)
SN74AS870 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	S0	13	DQB1
2	1A0	14	DQB2
3	1A1	15	DQB3
4	1A2	16	DQB4
5	1A3	17	S3
6	$1\overline{W}$	18	$2\overline{W}$
7	S2	19	2A0
8	DQA1	20	2A1
9	DQA2	21	2A2
10	DQA3	22	2A3
11	DQA4	23	S1
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	S0	16	DQB1
3	1A0	17	DQB2
4	1A1	18	DQB3
5	1A2	19	DQB4
6	1A3	20	S3
7	$1\overline{W}$	21	$2\overline{W}$
8	nc	22	nc
9	S2	23	2A0
10	DQA1	24	2A1
11	DQA2	25	2A2
12	DQA3	26	2A3
13	DQA4	27	S1
14	GND	28	V_{CC}

†Pin numbers shown on logic symbols are for JT and NT packages only.

nc — no internal connection.

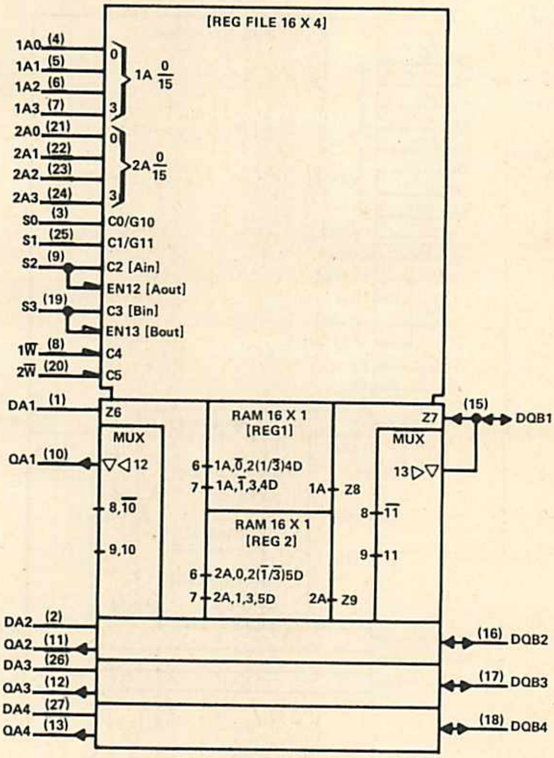
871

DUAL 16-BY-4 REGISTER FILES

- Each register file has individual write/enable controls and address lines
- Has one 4-bit data I/O port; the other 4-bit data word has individual data inputs and data outputs
- 28-pin, 600-mil package

SN54AS871 (J,FH)
SN74AS871 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES			
1	DA1	15	DQB1
2	DA2	16	DQB2
3	S0	17	DQB3
4	1A0	18	DQB4
5	1A1	19	S3
6	1A2	20	$\overline{2W}$
7	1A3	21	2A0
8	$\overline{1W}$	22	2A1
9	S2	23	2A2
10	QA1	24	2A3
11	QA2	25	S1
12	QA3	26	DA3
13	QA4	27	DA4
14	GND	28	V_{CC}

FH, FN PACKAGES			
1	DA1	15	DQB1
2	DA2	16	DQB2
3	S0	17	DQB3
4	1A0	18	DQB4
5	1A1	19	S3
6	1A2	20	$\overline{2W}$
7	1A3	21	2A0
8	$\overline{1W}$	22	2A1
9	S2	23	2A2
10	QA1	24	2A3
11	QA2	25	S1
12	QA3	26	DA3
13	QA4	27	DA4
14	GND	28	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

873

DUAL 4-BIT D-TYPE LATCHES

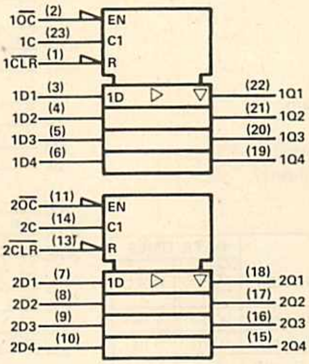
- Three-state buffer-type outputs drive bus lines directly
- Each 4-bit word has enable, clear, and output control inputs

typical performance

TYPE	CLEAR	OUTPUT	DELAY	POWER
'ALS873	LOW	Q	11 ns	67.5 mW
'AS873	LOW	Q	4.5 ns	358 mW

SN54ALS873(JT,FH) SN74ALS873 (NT,FN)
SN54AS873 (JT,FH) SN74AS873 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	$1\overline{CLR}$	13	$2\overline{CLR}$
2	$1\overline{OC}$	14	2C
3	1D1	15	2Q4
4	1D2	16	2Q3
5	1D3	17	2Q2
6	1D4	18	2Q1
7	2D1	19	1Q4
8	2D2	20	1Q3
9	2D3	21	1Q2
10	2D4	22	1Q1
11	$2\overline{OC}$	23	1C
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$1\overline{CLR}$	16	$2\overline{CLR}$
3	$1\overline{OC}$	17	2C
4	1D1	18	2Q4
5	1D2	19	2Q3
6	1D3	20	2Q2
7	1D4	21	2Q1
8	nc	22	nc
9	2D1	23	1Q4
10	2D2	24	1Q3
11	2D3	25	1Q2
12	2D4	26	1Q1
13	$2\overline{OC}$	27	1C
14	GND	28	V_{CC}

874

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- Three-state buffer-type outputs
- Each 4-bit word has clock, clear, and output control inputs

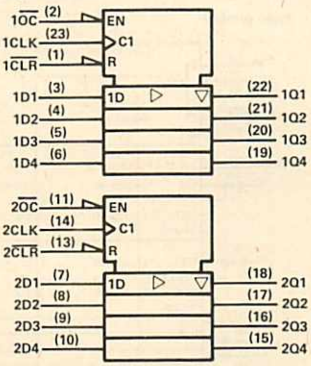
typical performance

TYPE	FREQ	POWER	DATA TIMES	
			SET-UP	HOLD
SN54ALS874	50 MHz	86.7 mW	10 ns↑	4 ns↑
SN74ALS874	50 MHz	86.7 mW	10 ns↑	4 ns↑
SN54AS874	175 MHz	456 mW	5 ns↑	1 ns↑
SN54AS874	175 MHz	456 mW	4 ns↑	1 ns↑

↑ Rising edge of clock pulse

SN54ALS874 (JT,FH) SN74ALS874 (NT,FN)
SN54AS874 (JT,FH) SN74AS874 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	$1\overline{CLR}$	13	$2\overline{CLR}$
2	$1\overline{OC}$	14	2CLK
3	1D1	15	2Q4
4	1D2	16	2Q3
5	1D3	17	2Q2
6	1D4	18	2Q1
7	2D1	19	1Q4
8	2D2	20	1Q3
9	2D3	21	1Q2
10	2D4	22	1Q1
11	$2\overline{OC}$	23	1CLK
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$1\overline{CLR}$	16	$2\overline{CLR}$
3	$1\overline{OC}$	17	2CLK
4	1D1	18	2Q4
5	1D2	19	2Q3
6	1D3	20	2Q2
7	1D4	21	2Q1
8	nc	22	nc
9	2D1	23	1Q4
10	2D2	24	1Q3
11	2D3	25	1Q2
12	2D4	26	1Q1
13	$2\overline{OC}$	27	1CLK
14	GND	28	V_{CC}

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†Pin numbers shown on logic symbols are for JT and NT packages only.

nc — no internal connection.

876

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH INVERTED OUTPUTS

- Three-state buffer-type outputs drive bus lines directly
- Each 4-bit word has own clock, preset, and output control inputs

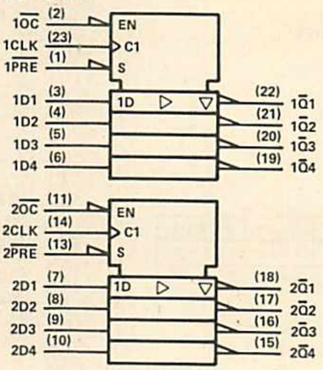
typical performance

TYPE	FREQ	POWER	DATA TIMES	
			SET-UP	HOLD
SN54ALS876	50 MHz	86.7 mW	10 ns†	4 ns†
SN74ALS876	50 MHz	86.7 mW	10 ns†	0 ns†
SN54AS876	175 MHz	470 mW	5 ns†	1 ns†
SN74AS876	175 MHz	470 mW	4 ns†	1 ns†

† Rising edge of clock pulse

SN54ALS876 (JT,FH) SN74ALS876 (NT,FN)
SN54AS876 (JT,FH) SN74AS876 (NT,FN)

logic symbol†



$1\overline{\text{OC}}$ (2)
1CLK (23)
$1\overline{\text{PRE}}$ (1)
EN
C1
S
1D1 (3)
1D2 (4)
1D3 (5)
1D4 (6)
1D
(22) $1\overline{\text{Q}}1$
(21) $1\overline{\text{Q}}2$
(20) $1\overline{\text{Q}}3$
(19) $1\overline{\text{Q}}4$
$2\overline{\text{OC}}$ (11)
2CLK (14)
$2\overline{\text{PRE}}$ (13)
EN
C1
S
2D1 (7)
2D2 (8)
2D3 (9)
2D4 (10)
1D
(18) $2\overline{\text{Q}}1$
(17) $2\overline{\text{Q}}2$
(16) $2\overline{\text{Q}}3$
(15) $2\overline{\text{Q}}4$

pin assignments

JT, NT PACKAGES			
1	$1\overline{\text{PRE}}$	13	$2\overline{\text{PRE}}$
2	$1\overline{\text{OC}}$	14	2CLK
3	1D1	15	$2\overline{\text{Q}}4$
4	1D2	16	$2\overline{\text{Q}}3$
5	1D3	17	$2\overline{\text{Q}}2$
6	1D4	18	$2\overline{\text{Q}}1$
7	2D1	19	$1\overline{\text{Q}}4$
8	2D2	20	$1\overline{\text{Q}}3$
9	2D3	21	$1\overline{\text{Q}}2$
10	2D4	22	$1\overline{\text{Q}}1$
11	$2\overline{\text{OC}}$	23	1CLK
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$1\overline{\text{PRE}}$	16	$2\overline{\text{PRE}}$
3	$1\overline{\text{OC}}$	17	2CLK
4	1D1	18	$2\overline{\text{Q}}4$
5	1D2	19	$2\overline{\text{Q}}3$
6	1D3	20	$2\overline{\text{Q}}2$
7	1D4	21	$2\overline{\text{Q}}1$
8	nc	22	nc
9	2D1	23	$1\overline{\text{Q}}4$
10	2D2	24	$1\overline{\text{Q}}3$
11	2D3	25	$1\overline{\text{Q}}2$
12	2D4	26	$1\overline{\text{Q}}1$
13	$2\overline{\text{OC}}$	27	1CLK
14	GND	28	V_{CC}

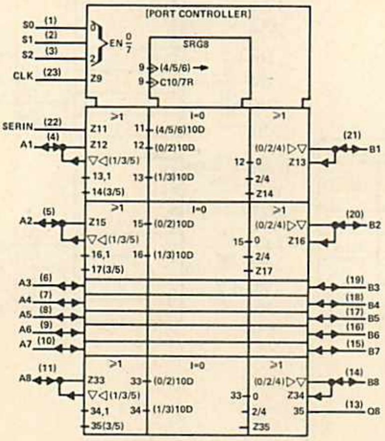
877

8-BIT UNIVERSAL TRANSCEIVER/PORT CONTROLLERS

- 8 selectable transceiver/port functions
- 3-state buffer-type outputs drive bus lines directly
- 24-pin 300-mil package

SN54AS877 (JT,FH)
SN74AS877 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES				FH, FN PACKAGES			
1	S0	13	Q8	1	nc	15	nc
2	S1	14	B8	2	S0	16	Q8
3	S2	15	B7	3	S1	17	B8
4	A1	16	B6	4	S2	18	B7
5	A2	17	B5	5	A1	19	B6
6	A3	18	B4	6	A2	20	B5
7	A4	19	B3	7	A3	21	B4
8	A5	20	B2	8	nc	22	nc
9	A6	21	B1	9	A4	23	B3
10	A7	22	SERIN	10	A5	24	B2
11	A8	23	CLK	11	A6	25	B1
12	GND	24	V_{CC}	12	A7	26	SERIN
				13	A8	27	CLK
				14	GND	28	V_{CC}

†Pin numbers shown on logic symbols are for JT and NT packages only.
nc — no internal connection.

878

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- Three-state buffer-type outputs
- Each 4-bit word has clock, clear, and output control inputs

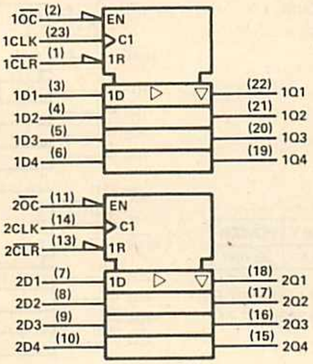
typical performance

TYPE	FREQ	POWER	DATA TIMES	
			SET-UP	HOLD
SN54ALS878	50 MHz	86.7 mW	10 ns†	4 ns†
SN74ALS878	50 MHz	86.7 mW	10 ns†	0 ns†
SN54AS878	175 MHz	463 mW	3 ns†	3 ns†
SN74AS878	175 MHz	463 mW	2 ns†	2 ns†

†Rising edge of clock pulse

SN54ALS878 (JT,FH) SN74ALS878 (NT,FN)
SN54AS878 (JT,FH) SN74AS878 (NT,FN)

logic symbol, 'ALS878, 'AS878†



pin assignments

JT, NT PACKAGES			
1	1$\overline{\text{CLR}}$	13	2$\overline{\text{CLR}}$
2	1$\overline{\text{OC}}$	14	2CLK
3	1D1	15	2Q4
4	1D2	16	2Q3
5	1D3	17	2Q2
6	1D4	18	2Q1
7	2D1	19	1Q4
8	2D2	20	1Q3
9	2D3	21	1Q2
10	2D4	22	1Q1
11	2$\overline{\text{OC}}$	23	1CLK
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	1$\overline{\text{CLR}}$	16	2$\overline{\text{CLR}}$
3	1$\overline{\text{OC}}$	17	2CLK
4	1D1	18	2Q4
5	1D2	19	2Q3
6	1D3	20	2Q2
7	1D4	21	2Q1
8	nc	22	nc
9	2D1	23	1Q4
10	2D2	24	1Q3
11	2D3	25	1Q2
12	2D4	26	1Q1
13	2$\overline{\text{OC}}$	27	1CLK
14	GND	28	V_{CC}

879

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH INVERTED OUTPUTS

- Three state buffer-type outputs
- Each 4-bit word has clock, clear, and output control inputs.

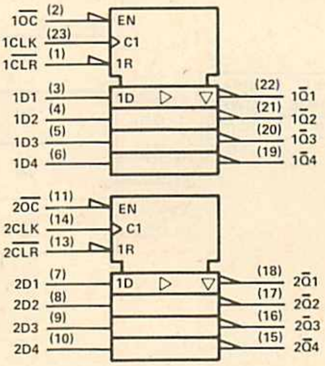
typical performance

TYPE	FREQ	POWER	DATA TIMES	
			SET-UP	HOLD
SN54ALS879	50 MHz	86.7 mW	10 ns†	4 ns†
SN74ALS879	50 MHz	86.7 mW	10 ns†	0 ns†
SN54AS879	175 MHz	470 mW	3 ns†	3 ns†
SN74AS879	175 MHz	470 mW	2 ns†	2 ns†

†Rising edge of clock pulse

SN54ALS879 (JT,FH) SN74ALS879 (NT,FN)
SN54AS879 (JT,FH) SN74AS879 (NT,FN)

logic symbol, 'ALS879, 'AS879†


1$\overline{\text{OC}}$ (2)
1CLK (23)
1$\overline{\text{CLR}}$ (1)
EN
C1
1R
1D1 (3)
1D2 (4)
1D3 (5)
1D4 (6)
1D
(22) 1$\overline{\text{Q}}$1
(21) 1$\overline{\text{Q}}$2
(20) 1$\overline{\text{Q}}$3
(19) 1$\overline{\text{Q}}$4
2$\overline{\text{OC}}$ (11)
2CLK (14)
2$\overline{\text{CLR}}$ (13)
EN
C1
1R
2D1 (7)
2D2 (8)
2D3 (9)
2D4 (10)
1D
(18) 2$\overline{\text{Q}}$1
(17) 2$\overline{\text{Q}}$2
(16) 2$\overline{\text{Q}}$3
(15) 2$\overline{\text{Q}}$4

pin assignments

JT, NT PACKAGES			
1	1$\overline{\text{CLR}}$	13	2$\overline{\text{CLR}}$
2	1$\overline{\text{OC}}$	14	2CLK
3	1D1	15	2$\overline{\text{Q}}$4
4	1D2	16	2$\overline{\text{Q}}$3
5	1D3	17	2$\overline{\text{Q}}$2
6	1D4	18	2$\overline{\text{Q}}$1
7	2D1	19	1$\overline{\text{Q}}$4
8	2D2	20	1$\overline{\text{Q}}$3
9	2D3	21	1$\overline{\text{Q}}$2
10	2D4	22	1$\overline{\text{Q}}$1
11	2$\overline{\text{OC}}$	23	1CLK
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	1$\overline{\text{CLR}}$	16	2CLR
3	1$\overline{\text{OC}}$	17	2CLK
4	1D1	18	2$\overline{\text{Q}}$4
5	1D2	19	2$\overline{\text{Q}}$3
6	1D3	20	2$\overline{\text{Q}}$2
7	1D4	21	2$\overline{\text{Q}}$1
8	nc	22	nc
9	2D1	23	1$\overline{\text{Q}}$4
10	2D2	24	1$\overline{\text{Q}}$3
11	2D3	25	1$\overline{\text{Q}}$2
12	2D4	26	1$\overline{\text{Q}}$1
13	2$\overline{\text{OC}}$	27	1CLK
14	GND	28	V_{CC}

---

†Pin numbers shown on logic symbols are for JT and NT packages only.

nc — no internal connection.

880

DUAL 4-BIT D-TYPE LATCHES WITH INVERTED OUTPUTS

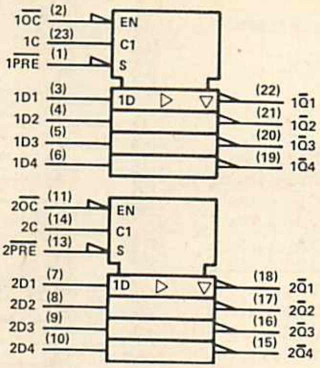
- Three-state buffer-type outputs drive bus lines directly
- Each 4-bit word has enable, preset, and output control inputs

typical performance

TYPE	OUTPUT	DELAY	POWER
'ALS880	$\overline{Q}$	11.5 ns	88 mW

SN54ALS880(JT,FH) SN74ALS880 (NT,FN)
SN54AS880 (JT,FH) SN74AS880 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	$1\overline{PRE}$	13	$2\overline{PRE}$
2	$1\overline{OC}$	14	2C
3	1D1	15	$2\overline{Q}4$
4	1D2	16	$2\overline{Q}3$
5	1D3	17	$2\overline{Q}2$
6	1D4	18	$2\overline{Q}1$
7	2D1	19	$1\overline{Q}4$
8	2D2	20	$1\overline{Q}3$
9	2D3	21	$1\overline{Q}2$
10	2D4	22	$1\overline{Q}1$
11	$2\overline{OC}$	23	1C
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$1\overline{PRE}$	16	$2\overline{PRE}$
3	$1\overline{OC}$	17	2C
4	1D1	18	$2\overline{Q}4$
5	1D2	19	$2\overline{Q}3$
6	1D3	20	$2\overline{Q}2$
7	1D4	21	$2\overline{Q}1$
8	nc	22	nc
9	2D1	23	$1\overline{Q}4$
10	2D2	24	$1\overline{Q}3$
11	2D3	25	$1\overline{Q}2$
12	2D4	26	$1\overline{Q}1$
13	$2\overline{OC}$	27	1C
14	GND	28	V_{CC}

881

ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS

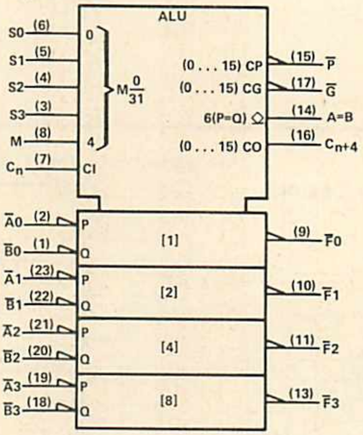
- 4-bit ALU's/Function Generators
- Same operating modes as 'AS181A, 'S181A expanded to include status register checks

typical performance

TYPE	CARRY TIME	16-BIT ADD TIME	TOTAL POWER
'AS881A	7.5 ns	20 ns	560 mW

SN54AS881A (JT,FH)
SN74AS881A (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	$\overline{B}0$	13	$\overline{F}3$
2	$\overline{A}0$	14	A=B
3	S3	15	$\overline{P}$
4	S2	16	C_{n+4}
5	S1	17	$\overline{G}$
6	S0	18	$\overline{B}3$
7	C_n	19	$\overline{A}3$
8	M	20	$\overline{B}2$
9	$\overline{F}0$	21	$\overline{A}2$
10	$\overline{F}1$	22	$\overline{B}1$
11	$\overline{F}2$	23	$\overline{A}1$
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$\overline{B}0$	16	$\overline{F}3$
3	$\overline{A}0$	17	A=B
4	S3	18	$\overline{P}$
5	S2	19	C_{n+4}
6	S1	20	$\overline{G}$
7	S0	21	$\overline{B}3$
8	nc	22	nc
9	C_n	23	$\overline{A}3$
10	M	24	$\overline{B}2$
11	$\overline{F}0$	25	$\overline{A}2$
12	$\overline{F}1$	26	$\overline{B}1$
13	$\overline{F}2$	27	$\overline{A}1$
14	GND	28	V_{CC}

---

†Pin numbers shown on logic symbols are for JT and NT packages only.

nc – no internal connection.

882

32-BIT LOOK-AHEAD CARRY GENERATORS

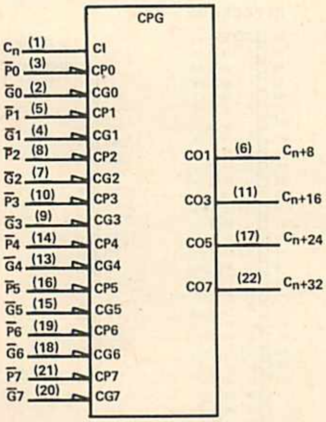
- Directly compatible with 'AS181, 'AS881, and 'S181 ALU's

typical performance

TYPE	CARRY TIME	TOTAL POWER
'AS882	8 ns	325 mW

SN54AS882 (JT,FH)
SN74AS882 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	C_n	13	$\overline{G4}$
2	$\overline{G0}$	14	$\overline{P4}$
3	$\overline{P0}$	15	$\overline{G5}$
4	$\overline{G1}$	16	$\overline{P5}$
5	$\overline{P1}$	17	C_{n+24}
6	C_{n+8}	18	$\overline{G6}$
7	$\overline{G2}$	19	$\overline{P6}$
8	P2	20	$\overline{G7}$
9	$\overline{G3}$	21	$\overline{P7}$
10	$\overline{P3}$	22	C_{n+32}
11	C_{n+16}	23	nc
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	C_n	16	$\overline{G4}$
3	$\overline{G0}$	17	$\overline{P4}$
4	$\overline{P0}$	18	$\overline{G5}$
5	$\overline{G1}$	19	$\overline{P5}$
6	$\overline{P1}$	20	C_{n+24}
7	C_{n+8}	21	$\overline{G6}$
8	nc	22	nc
9	$\overline{G2}$	23	$\overline{P6}$
10	$\overline{P2}$	24	$\overline{G7}$
11	$\overline{G3}$	25	$\overline{P7}$
12	$\overline{P3}$	26	C_{n+32}
13	C_{n+16}	27	nc
14	GND	28	V_{CC}

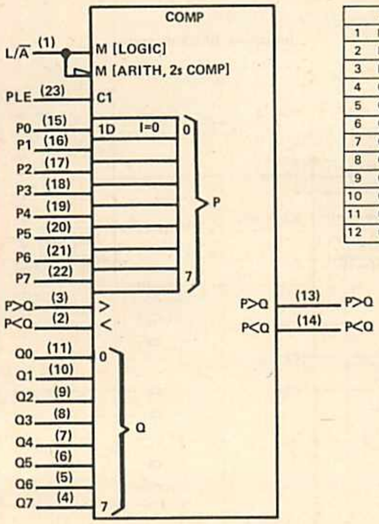
885

8-BIT MAGNITUDE COMPARATORS

- Choice of logical or arithmetic comparisons
- Latchable P input ports; power clear

SN54AS885 (JT,FH)
SN74AS885 (NT,FN)

logic symbol†



pin assignments

JT, NT PACKAGES			
1	$L/\overline{A}$	13	P>Qout
2	P<Qin	14	P<Qout
3	P>Qin	15	P0
4	Q7	16	P1
5	Q6	17	P2
6	Q5	18	P3
7	Q4	19	P4
8	Q3	20	P5
9	Q2	21	P6
10	Q1	22	P7
11	Q0	23	PLE
12	GND	24	V_{CC}

FH, FN PACKAGES			
1	nc	15	nc
2	$L/\overline{A}$	16	P>Qout
3	P<Qin	17	P<Qout
4	P>Qin	18	P0
5	Q7	19	P1
6	Q6	20	P2
7	Q5	21	P3
8	nc	22	nc
9	Q4	23	P4
10	Q3	24	P5
11	Q2	25	P6
12	Q1	26	P7
13	Q0	27	PLE
14	GND	28	V_{CC}

†Pin numbers shown on logic symbols are for JT and NT packages only.
nc – no internal connection.

888, 889

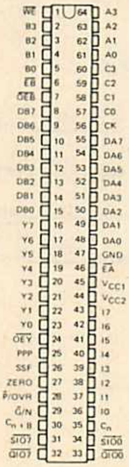
8-BIT PROCESSOR SLICES

- STL-AS technology
- Parallel 8-bit ALU with expansion inputs and outputs
- 13 arithmetic and logic functions
- 8 conditional shifts (single and double length)
- 9 instructions that manipulate bytes
- 4 instructions that manipulate bits
- Add and subtract immediate instructions
- Absolute value instruction
- Signed magnitude to/from 2's complement conversion
- Polynomial code accumulation (CRC, FIRE, Computer Generated, etc.)
- Single- and double-length normalize
- Select functions
- Signed and unsigned divides with overflow detection; input does not need to be prescaled
- Signed, mixed, and unsigned multiples
- Three-operand, 16-word register file
- Full carry look ahead support
- Sign, carry out, overflow, and zero-detect status capabilities
- Excess-3 BCD arithmetic

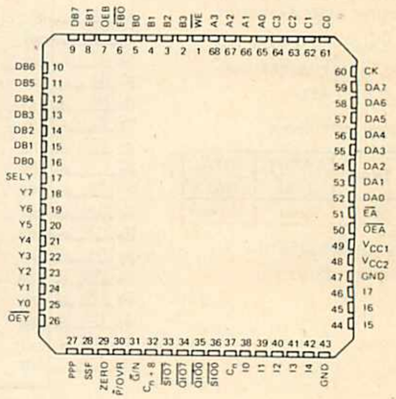
SN54AS888 (JD)	SN74AS888 (JD)
SN54AS889 (FN)	SN74AS889 (FN)

pin assignments

JD PACKAGE

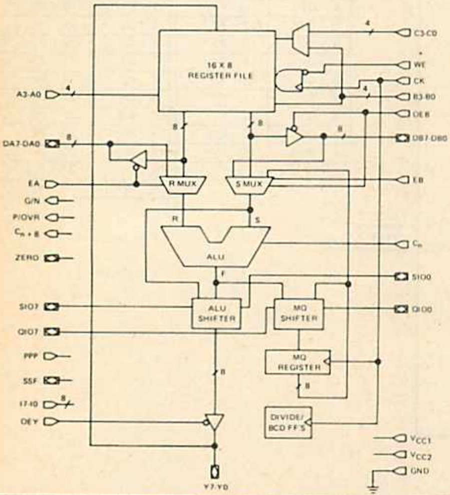


FN PACKAGE

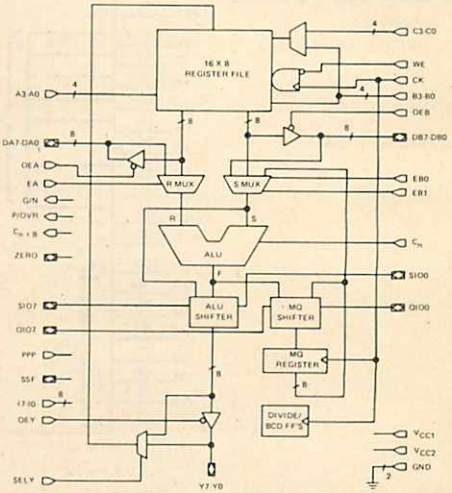


functional block diagram

'AS888



'AS889



890, 891

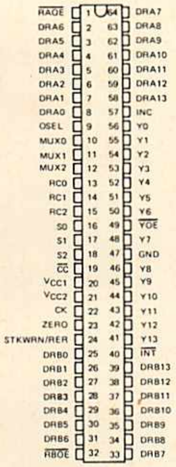
MICROSEQUENCERS

- 14 bits wide — Addresses up to 16,384 words of microcode with one chip
- *Selects address* from one of eight sources
- STL-AS technology
- Independent read pointer for aid in micro-code diagnostics
- Supports real-time interrupts
- Two independent loop counters
- Supports 64 powerful instructions

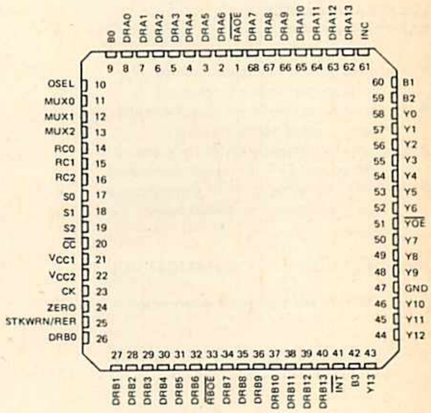
SN54AS890 (JD)	SN74AS890 (JD)
SN54AS891 (FN)	SN74AS891 (FN)

pin assignments

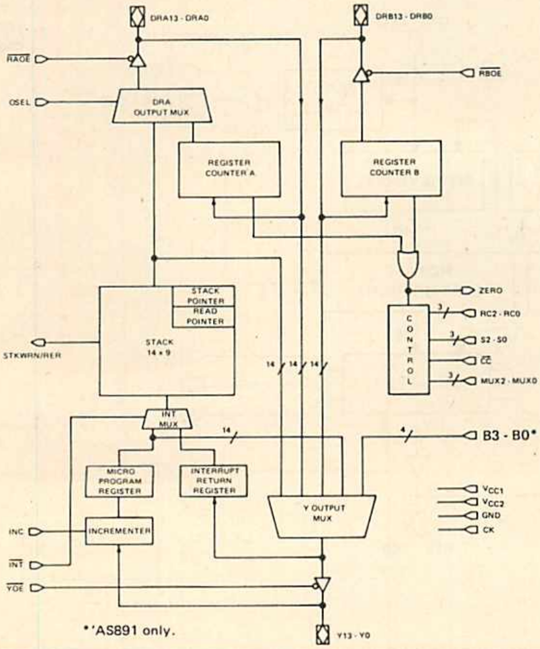
JD PACKAGE



FN PACKAGE



functional block diagram



*'AS891 only.

897

16-BIT EXPANDABLE BARREL SHIFTER

- Performs arithmetic, logical, and circular shifts on data in one clock cycle
- Performs bit set and reset operations and floating point normalizations
- Contains an internal counter for memory address and FFT bit reverse addressing
- Ideal for improving the shift throughout on a microprocessor or AS888 based system

SN54AS897 (JD) SN74AS897 (JD)

Contact factory for additional information

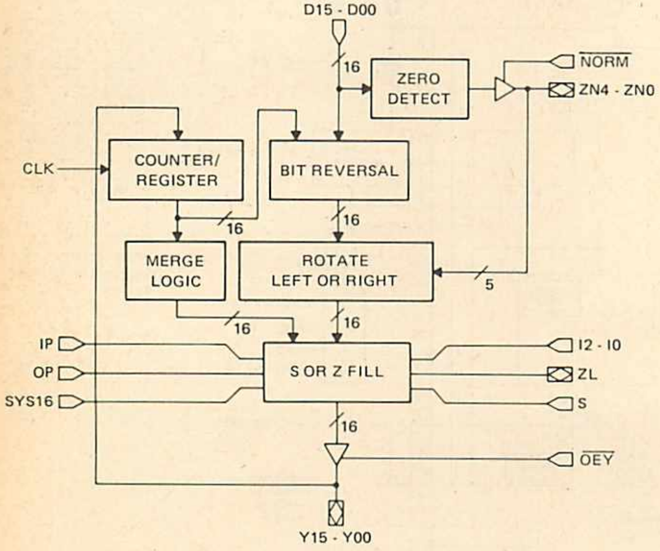
pin assignments

JD, N PACKAGES	
1 ZN3	27 $V_{CC}2$
2 ZN2	28 I0
3 ZN1	29 I1
4 ZN0	30 I2
5 D15	31 CLK
6 D14	32 Y0
7 D13	33 Y1
8 D12	34 Y2
9 D11	35 Y3
10 D10	36 Y4
11 D9	37 Y5
12 D8	38 Y6
13 GND	39 Y7
14 D7	40 GND
15 D6	41 Y8
16 D5	42 Y9
17 D4	43 Y10
18 D3	44 Y11
19 D2	45 Y12
20 D1	46 Y13
21 D0	47 Y14
22 IP	48 Y15
23 OP	49 $\overline{\text{OEY}}$
24 SYS16	50 $\overline{\text{NORM}}$
25 ZL	51 ZN4
26 S	52 $V_{CC}1$

For chip carrier information, contact the factory.

AS897 16-BIT EXPANDABLE BARREL SHIFTER

functional block diagram



1000

QUAD 2-INPUT NAND BUFFERS/DRIVERS

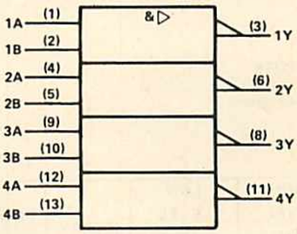
- *Increased* output drive capability over 'LS00, 'ALS00, 'AS00

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/ GATE
SN54ALS1000A	12 mA	– 1 mA	4 ns	3 mW
SN74ALS1000A	24 mA	– 2.6 mA	4 ns	3 mW
SN54AS1000	40 mA	– 40 mA	1.7 ns	8.6 mW
SN74AS1000	48 mA	– 48 mA	1.7 ns	8.6 mW

SN54ALS1000A (J,FH) SN74ALS1000A (N,FN)
SN54AS1000 (J,FH) SN74AS1000 (N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	nc	15	nc
6	2A	16	4Y
7	nc	17	nc
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

1002

QUAD 2-INPUT NOR BUFFER GATES

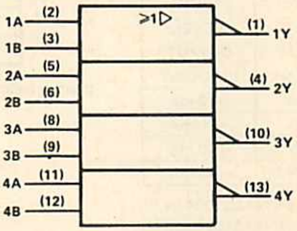
- Increased output drive capability over 'LS02.

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	DELAY	POWER/ GATE
SN54ALS1002A	12 mA	– 1 mA	4 ns	4 mW
SN74ALS1002A	24 mA	– 2.6 mA	4 ns	4 mW

SN54ALS1002A (J,FH) SN74ALS1002A (N,FN)

logic symbol†



positive logic: $Y = \overline{A+B}$

pin assignments

J, N PACKAGES			
1	1Y	8	3A
2	1A	9	3B
3	1B	10	3Y
4	2Y	11	4A
5	2A	12	4B
6	2B	13	4Y
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1Y	12	3A
3	1A	13	3B
4	1B	14	3Y
5	nc	15	nc
6	2Y	16	4A
7	nc	17	nc
8	2A	18	4B
9	2B	19	4Y
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

1003

QUAD 2-INPUT NAND BUFFER GATES WITH OPEN-COLLECTOR OUTPUTS

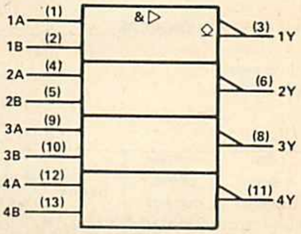
- Increased drive capability over 'LS03

typical performance

TYPE	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	DELAY	POWER/ GATE
SN54ALS1003A	5.5 V	12 mA	14.5 ns	3 mW
SN74ALS1003A	5.5 V	24 mA	14.5 ns	3 mW

SN54ALS1003A (J,FH) SN74ALS1003A (N,FN)

logic symbol†



positive logic: $Y = \overline{AB}$

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	nc	15	nc
6	2A	16	4Y
7	nc	17	nc
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

1004

HEX DRIVERS

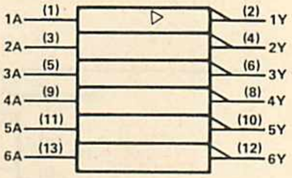
- Increased drive capability over LS04, ALS04, AS04

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1004	12 mA	− 12 mA
SN74ALS1004	24 mA	− 15 mA
SN54AS1004	40 mA	− 40 mA
SN74AS1004	48 mA	− 48 mA

SN54ALS1004 (J,FH) SN74ALS1004 (N,FN)
SN54AS1004 (J,FH) SN74AS1004 (N,FN)

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2A	14	5Y
5	nc	15	nc
6	2Y	16	5A
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

1005

HEX INVERTER BUFFER GATES WITH OPEN-COLLECTOR OUTPUTS

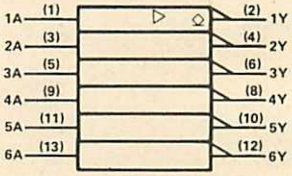
- Increased drive capability over LS05

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1005	12 mA	−1 mA
SN74ALS1005	24 mA	−2.6 mA

SN54ALS1005 (J,FH) SN74ALS1005 (N,FN)

logic symbol†



positive logic: $Y = \overline{A}$

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2A	14	5Y
5	nc	15	nc
6	2Y	16	5A
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

1008

QUADRUPLE 2-INPUT POSITIVE-AND BUFFERS/DRIVERS

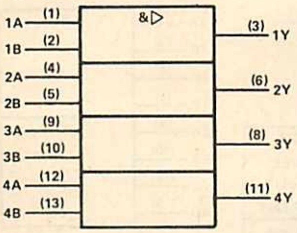
- Increased drive capability over LS08, ALS08, AS08

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1008A	12 mA	− 1 mA
SN74ALS1008A	24 mA	− 2.6 mA
SN54AS1008	40 mA	− 40 mA
SN74AS1008	48 mA	− 48 mA

SN54ALS1008A (J,FH) SN74ALS1008A (N,FN)
SN54AS1008 (J,FH) SN74AS1008 (N,FN)

logic symbol†



positive logic: Y = AB

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	nc	15	nc
6	2A	16	4Y
7	nc	17	nc
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

1010

TRIPLE 3-INPUT POSITIVE-NAND BUFFER GATES

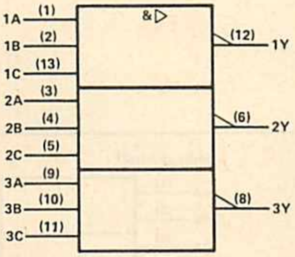
- Increased drive capability over LS10

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1010A	12 mA	− 1 mA
SN74ALS1010A	24 mA	− 2.6 mA

SN54ALS1010A (J,FH) SN74ALS1010A (N,FN)

logic symbol†



positive logic: Y = $\overline{ABC}$

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	2A	10	3B
4	2B	11	3C
5	2C	12	1Y
6	2Y	13	1C
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	2A	14	3B
5	nc	15	nc
6	2B	16	3C
7	nc	17	nc
8	2C	18	1Y
9	2Y	19	1C
10	GND	20	V_{CC}

1011

TRIPLE 3-INPUT POSITIVE-AND BUFFER GATES

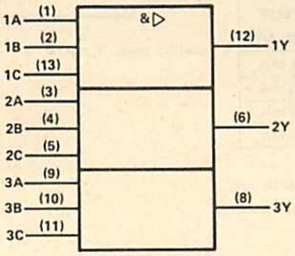
- Increased drive capability over LS11

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1011A	12 mA	− 1 mA
SN74ALS1011A	24 mA	− 2.6 mA

SN54ALS1011A (J,FH) SN74ALS1011A (N,FN)

logic symbol†



positive logic: Y = ABC

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	2A	10	3B
4	2B	11	3C
5	2C	12	1Y
6	2Y	13	1C
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	2A	14	3B
5	nc	15	nc
6	2B	16	3C
7	nc	17	nc
8	2C	18	1Y
9	2Y	19	1C
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

1020

DUAL 4-INPUT NAND BUFFER GATES

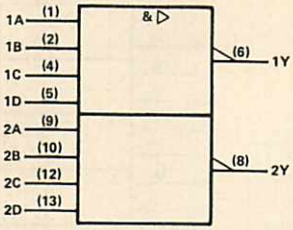
- Increased drive capability over LS20

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1020A	12 mA	− 1 mA
SN74ALS1020A	24 mA	− 2.6 mA

SN54ALS1020A (J,FH) SN74ALS1020A (N,FN)

logic symbol†



positive logic: $Y = \overline{ABCD}$

pin assignments

J, N PACKAGES			
1	1A	8	2Y
2	1B	9	2A
3	nc	10	2B
4	1C	11	nc
5	1D	12	2C
6	1Y	13	2D
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	2Y
3	1B	13	2A
4	nc	14	2B
5	nc	15	nc
6	1C	16	nc
7	nc	17	nc
8	1D	18	2C
9	1Y	19	2D
10	GND	20	V_{CC}

1032

QUADRUPLE 2-INPUT POSITIVE-OR BUFFER GATE

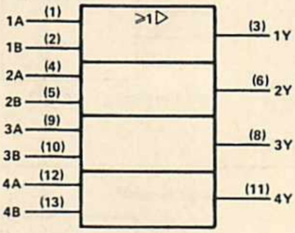
- Increased drive capability over LS32, ALS32, AS32

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1032A	12 mA	− 1 mA
SN74ALS1032A	24 mA	− 2.6 mA
SN54AS1032	40 mA	− 40 mA
SN74AS1032	48 mA	− 48 mA

SN54ALS1032A (J,FH) SN74ALS1032A (N,FN)
SN54AS1032 (J,FH) SN74AS1032 (N,FN)

logic symbol†



positive logic: $Y = A+B$

pin assignments

J, N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	nc	15	nc
6	2A	16	4Y
7	nc	17	nc
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

---

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

1034

HEX DRIVERS

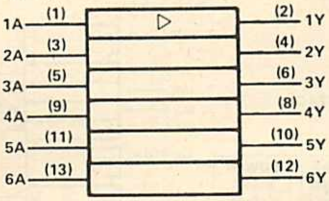
- Non-inverting outputs

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54ALS1034	12 mA	– 12 mA
SN74ALS1034	24 mA	– 15 mA
SN54AS1034	40 mA	– 40 mA
SN74AS1034	48 mA	– 48 mA

SN54ALS1034 (J,FH) SN74ALS1034 (N,FN)
SN54AS1034 (J,FH) SN74AS1034 (N,FN)

logic symbol†



positive logic Y = A

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2A	14	5Y
5	nc	15	nc
6	2Y	16	5A
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

1035

HEX BUFFERS WITH OPEN-COLLECTOR OUTPUTS

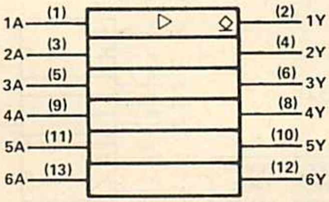
- Non-inverting outputs

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT VOLTAGE
SN54ALS1035	12 mA	5.5 V
SN74ALS1035	24 mA	5.5 V

SN54ALS1035 (J,FH) SN74ALS1035 (N,FN)

logic symbol†



Positive logic Y = A

pin assignments

J, N PACKAGES			
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

FH, FN PACKAGES			
1	nc	11	nc
2	1A	12	4Y
3	1Y	13	4A
4	2A	14	5Y
5	nc	15	nc
6	2Y	16	5A
7	nc	17	nc
8	3A	18	6Y
9	3Y	19	6A
10	GND	20	V_{CC}

1036

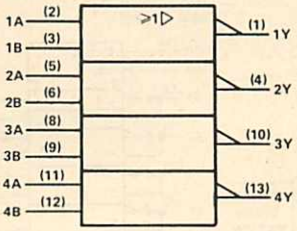
QUADRUPLE 2-INPUT POSITIVE NOR DRIVERS

- Quad version of 'AS805A

typical performance

TYPE	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT
SN54AS1036	40 mA	– 40 mA
SN74AS1036	48 mA	– 48 mA

logic symbol†



positive logic: $Y = \overline{A+B}$

pin assignments

J,N PACKAGES			
1	1A	8	3Y
2	1B	9	3A
3	1Y	10	3B
4	2A	11	4Y
5	2B	12	4A
6	2Y	13	4B
7	GND	14	V_{CC}

FH,FN PACKAGES			
1	nc	11	nc
2	1A	12	3Y
3	1B	13	3A
4	1Y	14	3B
5	nc	15	nc
6	2A	16	4Y
7	nc	17	nc
8	2B	18	4A
9	2Y	19	4B
10	GND	20	V_{CC}

---

†Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

1240

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS
(inverted three-state outputs)

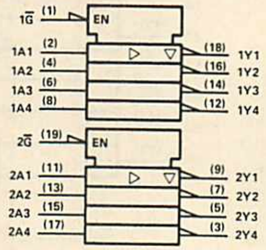
- Low power version of 'ALS240, AS240

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSI-PATION
SN54ALS1240	9	−12 mA	8 mA	47.5 mW
SN74ALS1240	9	−15 mA	16 mA	
SN74ALS1240-1	9	−15 mA	24 mA	

SN54ALS1240 (J,FH)　SN74ALS1240 (N, FN)
SN74ALS1240-1 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1$\overline{G}$	11	2A1	1	1$\overline{G}$	11	2A1
2	1A1	12	1Y4	2	1A1	12	1Y4
3	2Y4	13	2A2	3	2Y4	13	2A2
4	1A2	14	1Y3	4	1A2	14	1Y3
5	2Y3	15	2A3	5	2Y3	15	2A3
6	1A3	16	1Y2	6	1A3	16	1Y2
7	2Y2	17	2A4	7	2Y2	17	2A4
8	1A4	18	1Y1	8	1A4	18	1Y1
9	2Y1	19	2$\overline{G}$	9	2Y1	19	2$\overline{G}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

1241

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS
(non-inverted three-state outputs)

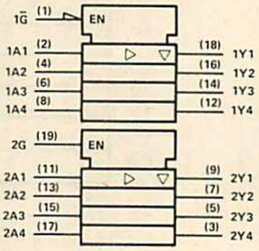
- Low power version of 'ASL241, LS241

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSI-PATION
SN54ALS1241	9	−12 mA	8 mA	47.5 mW
SN74ALS1241	9	−15 mA	16 mA	
SN74ALS1241-1	9	−15 mA	24 mA	

SN54ALS1241 (J,FH)　SN74ALS1241 (N,FN)
SN74ALS1241-1 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1$\overline{G}$	11	2A1	1	1$\overline{G}$	11	2A1
2	1A1	12	1Y4	2	1A1	12	1Y4
3	2Y4	13	2A2	3	2Y4	13	2A2
4	1A2	14	1Y3	4	1A2	14	1Y3
5	2Y3	15	2A3	5	2Y3	15	2A3
6	1A3	16	1Y2	6	1A3	16	1Y2
7	2Y2	17	2A4	7	2Y2	17	2A4
8	1A4	18	1Y1	8	1A4	18	1Y1
9	2Y1	19	2G	9	2Y1	19	2G
10	GND	20	V_{CC}	10	GND	20	V_{CC}

1242

QUADRUPLE BUS TRANSCEIVERS
(inverted three-state outputs)

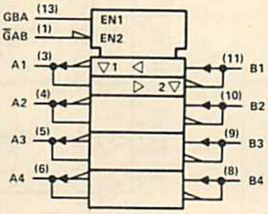
- Low power version of ALS242, LS242

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSI-PATION
SN54ALS1242		−12 mA	8 mA	
SN74ALS1242		−15 mA	16 mA	
SN74ALS1242-1		−15 mA	24 mA	

SN54ALS1242 (J,FH)　SN74ALS1242 (N, FN)
SN74ALS1242-1 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{G}$AB	8	B4	1	nc	11	nc
2	nc	9	B3	2	$\overline{G}$AB	12	B4
3	A1	10	B2	3	nc	13	B3
4	A2	11	B1	4	A1	14	B2
5	A3	12	nc	5	nc	15	nc
6	A4	13	GBA	6	A2	16	B1
7	GND	14	V_{CC}	7	nc	17	nc
				8	A3	18	nc
				9	A4	19	GBA
				10	GND	20	V_{CC}

†Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

1243

QUADRUPLE BUS TRANSCEIVERS
(non-inverted three-state outputs)

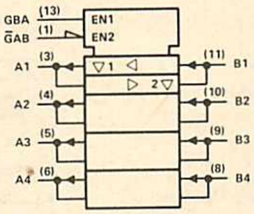
- Low power version of ALS243, LS243

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSI-PATION
SN54ALS1243		−12 mA	8 mA	
SN74ALS1243		−15 mA	16 mA	
SN74ALS1243-1		−15 mA	24 mA	

SN54ALS1243 (J,FH) SN74ALS1243 (N,FN)
SN74ALS1243-1 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$\overline{\mathrm{G}}$AB	8	B4	1	nc	11	nc
2	nc	9	B3	2	$\overline{\mathrm{G}}$AB	12	B4
3	A1	10	B2	3	nc	13	B3
4	A2	11	B1	4	A1	14	B2
5	A3	12	nc	5	nc	15	nc
6	A4	13	GBA	6	A2	16	B1
7	GND	14	V_{CC}	7	nc	17	nc
				8	A3	18	nc
				9	A4	19	GBA
				10	GND	20	V_{CC}

1244

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS
(non-inverted three-state outputs)

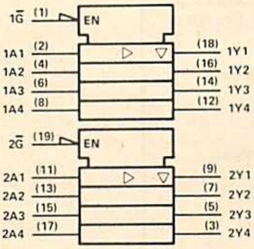
- Low power version of ALS244, LS244

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSI-PATION
SN54ALS1244A	9 ns	−12 mA	8 mA	
SN74ALS1244A	9 ns	−15 mA	16 mA	45 mW
SN74ALS1244A-1	9 ns	−15 mA	24 mA	

SN54ALS1244A (J,FH) SN74ALS1244A (N,FN)
SN74ALS1244A-1 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	1$\overline{\mathrm{G}}$	11	2A1	1	1$\overline{\mathrm{G}}$	11	2A1
2	1A1	12	1Y4	2	1A1	12	1Y4
3	2Y4	13	2A2	3	2Y4	13	2A2
4	1A2	14	1Y3	4	1A2	14	1Y3
5	2Y3	15	2A3	5	2Y3	15	2A3
6	1A3	16	1Y2	6	1A3	16	1Y2
7	2Y2	17	2A4	7	2Y2	17	2A4
8	1A4	18	1Y1	8	1A4	18	1Y1
9	2Y1	19	2$\overline{\mathrm{G}}$	9	2Y1	19	2$\overline{\mathrm{G}}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

1245

OCTAL BUS TRANSCEIVERS
(non-inverted three-state outputs)

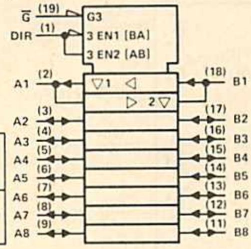
- Low power version of ALS245, LS245

typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT	POWER DISSI-PATION
SN54ALS1245	8	−12 mA	8 mA	
SN74ALS1245	8	−15 mA	16 mA	113 mW
SN74ALS1245-1	8	−15 mA	24 mA	

SN54ALS1245 (J,FH) SN74ALS1245 (N,FN)
SN74ALS1245-1 (N,FN)

logic symbol†



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	DIR	11	B8	1	DIR	11	B8
2	A1	12	B7	2	A1	12	B7
3	A2	13	B6	3	A2	13	B6
4	A3	14	B5	4	A3	14	B5
5	A4	15	B4	5	A4	15	B4
6	A5	16	B3	6	A5	16	B3
7	A6	17	B2	7	A6	17	B2
8	A7	18	B1	8	A7	18	B1
9	A8	19	$\overline{\mathrm{G}}$	9	A8	19	$\overline{\mathrm{G}}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

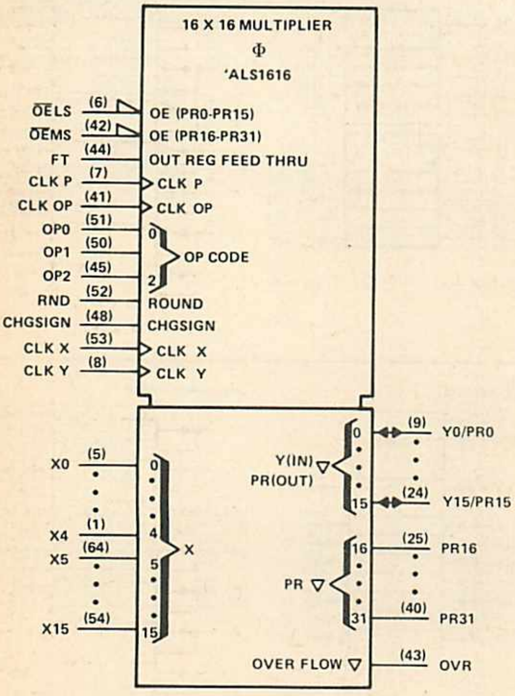
†Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

1616

16-×-16-BIT MULTIMODE MULTIPLIERS

- Multiplies Any Combination of Unsigned, Signed, Integer, or Fractional Inputs
- Registered Inputs and Outputs
- Comparable to TRW's MPY-16HJ
- Choice of Single-Signed, Double-Signed, Unsigned, or Signed Fractionally Adjusted Output
- Overflow Detected if a Combination of Input Data and/or Output Formats Result in a Number that Cannot be Represented
- Rounding is Provided for Both Integer and Fractional Results
- Flexible Input-Output Format Aids in Expansion to Multiple Precision Results
- 55 ns Typical Unclocked Multiply Time
- Power Dissipation Approximately 1.5 W
- 3-State Outputs
- Ideal for Signal Processing, Including Digital Filters, FFTs, and Automatic Line Integration
- Output may be Complemented
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

logic symbol



SN54ALS1616 (JD) SN74ALS1616 (JD)

pin assignments

JD PACKAGE			
1	X4	33	PR24
2	X3	34	PR25
3	X2	35	PR26
4	X1	36	PR27
5	X0	27	PR28
6	OELS	38	PR29
7	CLKP	39	PR30
8	CLKY	40	PR31
9	Y0/PR0	41	CLKOP
10	Y1/PR1	42	OEMS
11	Y2/PR2	43	OVR
12	Y3/PR3	44	FT
13	Y4/PR4	45	OP2
14	Y5/PR5	46	GND
15	Y6/PR6	47	GND
16	Y7/PR7	48	CHGSIGN
17	Y8/PR8	49	V_{CC}
18	Y9/PR9	50	OP1
19	Y10/PR10	51	OP0
20	Y11/PR11	52	RND
21	Y12/PR12	53	CLKX
22	Y13/PR13	54	X15
23	Y14/PR14	55	X14
24	Y15/PR15	56	X13
25	PR16	57	X12
26	PR17	58	X11
27	PR18	59	X10
28	PR19	60	X9
29	PR20	61	X8
20	PR21	62	X7
31	PR22	63	X6
32	PR23	64	X5

For chip carrier information, contact the factory.

1620, 1621, 1622, 1623

OCTAL BUS TRANSCEIVERS

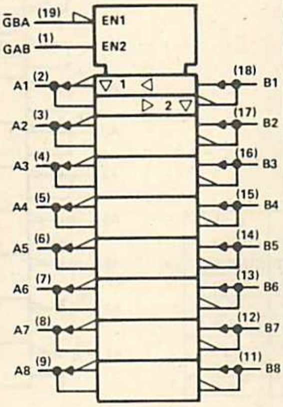
- Bidirectional bus transceivers
- Low power version of ALS 620, 621, 622, 623

typical performance

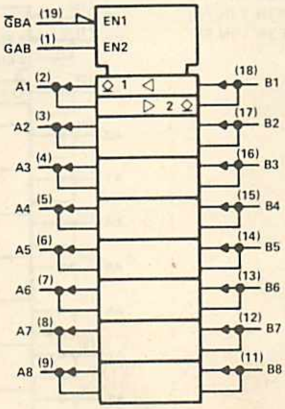
TYPE	OUTPUT	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS1620	3-State	−12	8 mA
SN74ALS1620	3-State	−15	16 mA
SN74ALS1620-1	3-State	−15	24 mA
SN54ALS1621	O-C	N/A	8 mA
SN74ALS1621	O-C	N/A	16 mA
SN74ALS1621-1	O-C	N/A	24 mA
SN54ALS1622	O-C	N/A	8 mA
SN74ALS1622	O-C	N/A	16 mA
SN74ALS1622-1	O-C	N/A	24 mA
SN54ALS1623	3-State	−12	8 mA
SN74ALS1623	3-State	−15	16 mA
SN74ALS1623-1	3-State	−15	24 mA

SN54ALS1620 (J,FH)	SN74ALS1620 (N,FN) SN74ALS1620-1 (N,FN)
SN54ALS1621 (J,FH)	SN74ALS1621 (N,FN) SN74ALS1621-1 (N,FN)
SN54ALS1622 (J,FH)	SN74ALS1622 (N,FN) SN74ALS1622-1 (N,FN)
SN54ALS1623 (J,FH)	SN74ALS1623 (N,FN) SN74ALS1623-1 (N,FN)

logic symbol, 'ALS1620†



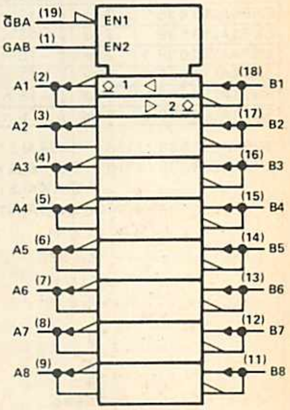
logic symbol, 'ALS1621†



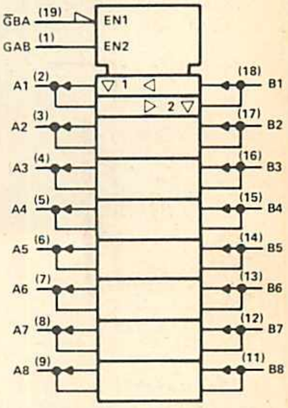
pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	GAB	11	B8	1	GAB	11	B8
2	A1	12	B7	2	A1	12	B7
3	A2	13	B6	3	A2	13	B6
4	A3	14	B5	4	A3	14	B5
5	A4	15	B4	5	A4	15	B4
6	A5	16	B3	6	A5	16	B3
7	A6	17	B2	7	A6	17	B2
8	A7	18	B1	8	A7	18	B1
9	A8	19	$\overline{\mathrm{G}}$BA	9	A8	19	$\overline{\mathrm{G}}$BA
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol, 'ALS1622†



logic symbol, 'ALS1623†



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†Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

1638, 1639

OCTAL BUS TRANSCEIVERS

- Bidirectional bus transceivers
- "A" bus outputs are open-collector: "B" bus outputs are three-state
- 'ALS1638—inverting logic
- 'ALS1639—true logic
- Low power versions of 'ALS638, 'ALS639

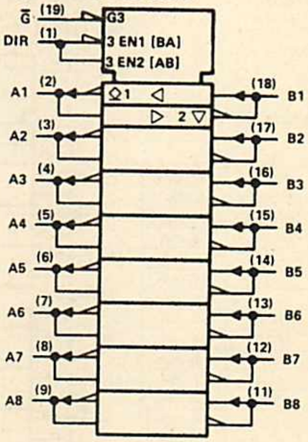
typical performance

TYPE	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS1638	7 ns	−12 mA	8 mA
SN74ALS1638	7 ns	−15 mA	16 mA
SN74ALS1638-1	7 ns	−15 mA	24 mA
SN54ALS1639	8 ns	−12 mA	8 mA
SN74ALS1639	8 ns	−15 mA	16 mA
SN74ALS1639-1	8 ns	−15 mA	24 mA

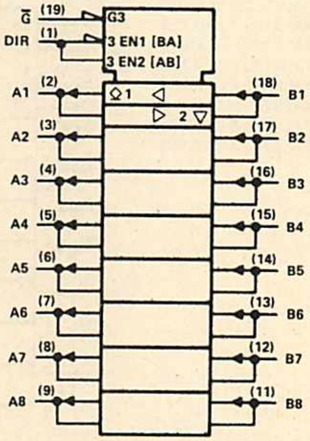
SN54ALS1638 (J,FH)
SN54ALS1639 (J,FH)

SN74ALS1638 (N,FN)
SN74ALS1639 (N,FN)
SN74ALS1638-1 (N,FN)
SN74ALS1639-1 (N,FN)

logic symbol, 'ALS1638†



logic symbol, 'ALS1639†



pin assignments

J, N PACKAGES			
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{G}$
10	GND	20	V_{CC}

FH, FN PACKAGES			
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{G}$
10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

1640, 1641, 1642, 1643, 1644, 1645

OCTAL BUS TRANSCEIVERS

- Low power versions of 'ALS640A, 'ALS641A, 'ALS642A, 'ALS643A, 'ALS644A, 'ALS645A

typical performance

TYPE	OUTPUT	DELAY	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54ALS1640A	3-State	7 ns	− 12 mA	8 mA
SN74ALS1640A	3-State	7 ns	− 15 mA	16 mA
SN74ALS1640A-1	3-State	7 ns	− 15 mA	24 mA
SN54ALS1641	O-C		N/A	8 mA
SN74ALS1641	O-C		N/A	16 mA
SN74ALS1641-1	O-C		N/A	24 mA
SN54ALS1642	O-C		N/A	8 mA
SN74ALS1642	O-C		N/A	16 mA
SN74ALS1642-1	O-C		N/A	24 mA
SN54ALS1643	3-State		− 12 mA	8 mA
SN74ALS1643	3-State		− 15 mA	16 mA
SN74ALS1643-1	3-State		− 15 mA	24 mA
SN54ALS1644	O-C		N/A	8 mA
SN74ALS1644	O-C		N/A	16 mA
SN74ALS1644-1	O-C		N/A	24 mA
SN54ALS645A	3-State	10 ns	− 12 mA	8 mA
SN74ALS645A	3-State	10 ns	− 15 mA	16 mA
SN74ALS645A-1	3-State	10 ns	− 15 mA	24 mA

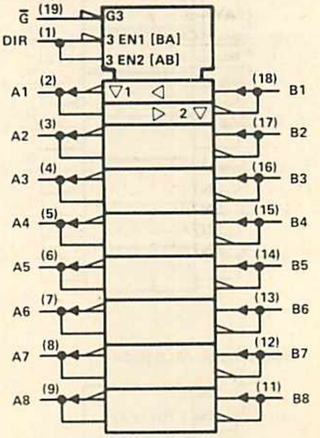
SN54ALS1640A (J,FH)
SN54ALS1641 (J,FH)
SN54ALS1642 (J,FH)
SN54ALS1643 (J,FH)
SN54ALS1644 (J,FH)
SN54ALS1645A (J,FH)

SN74ALS1640A (N,FN)
SN74ALS1641 (N,FN)
SN74ALS1642 (N,FN)
SN74ALS1643 (N,FN)
SN74ALS1644 (N,FN)
SN74ALS1645A (N,FN)
SN74ALS1640A-1 (N,FN)
SN74ALS1641-1 (N,FN)
SN74ALS1642-1 (N,FN)
SN74ALS1643-1 (N,FN)
SN74ALS1644-1 (N,FN)
SN74ALS1645A-1 (N,FN)

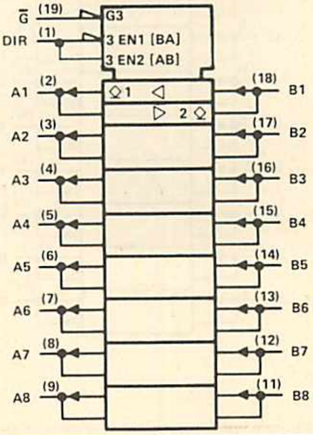
pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	DIR	11	B8	1	DIR	11	B8
2	A1	12	B7	2	A1	12	B7
3	A2	13	B6	3	A2	13	B6
4	A3	14	B5	4	A3	14	B5
5	A4	15	B4	5	A4	15	B4
6	A5	16	B3	6	A5	16	B3
7	A6	17	B2	7	A6	17	B2
8	A7	18	B1	8	A7	18	B1
9	A8	19	$\overline{G}$	9	A8	19	$\overline{G}$
10	GND	20	V_{CC}	10	GND	20	V_{CC}

logic symbol, 'ALS1640A†



logic symbol, 'ALS1641†

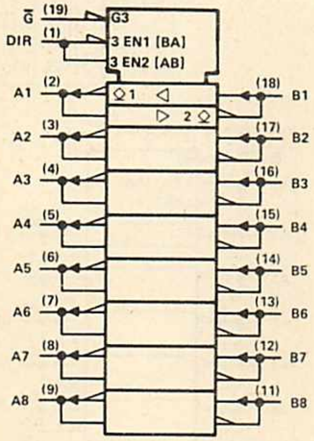


† Pin numbers shown on logic symbols are for J and N packages only.

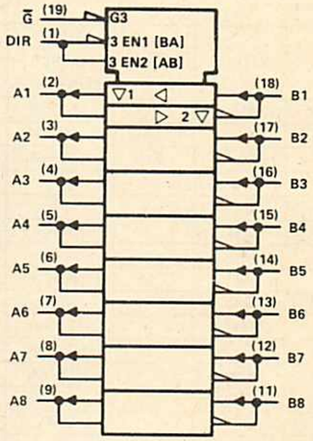
nc — no internal connection.

1640, 1641, 1642, 1643, 1644, 1645 continued

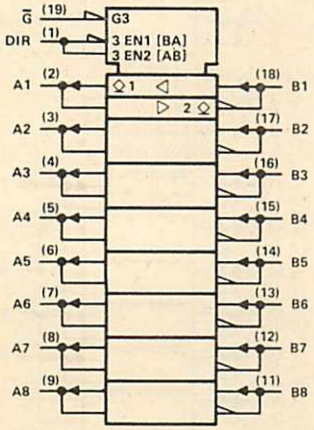
logic symbol, 'ALS1642†



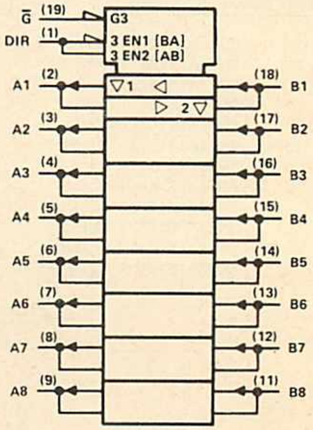
logic symbol, 'ALS1643†



logic symbol, 'ALS1644†



logic symbol, 'ALS1645A†



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†Pin numbers shown on logic symbols are for J and N packages only.

2620, 2623

OCTAL BUS TRANSCEIVERS/MOS DRIVERS

- Bidirectional bus transceivers for driving MOS devices
- Local bus latch capability
- I/O ports have 25 ohm series resistors so no external resistors are required
- Choice of True or Inverting logic
- 3-State outputs

typical performance

TYPE	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54AS2620	– 12 mA	48 mA
SN74AS2620	– 15 mA	64 mA
SN54AS2623	– 12 mA	48 mA
SN74AS2623	– 15 mA	64 mA

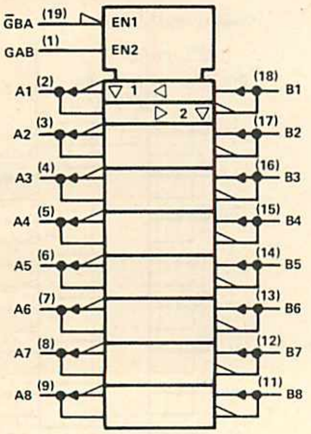
SN54AS2620 (J,FH) SN74AS2620 (N,FN)
SN54AS2623 (J,FH) SN74AS2623 (N,FN)

pin assignments

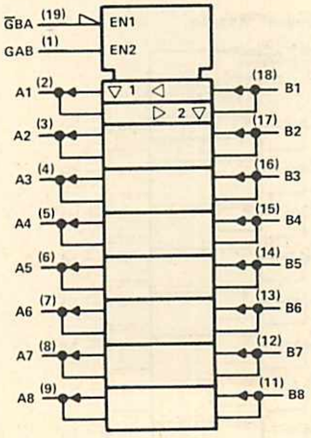
J,N PACKAGES			
1	GAB	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{\mathrm{GBA}}$
10	GND	20	V_{CC}

FH,FN PACKAGES			
1	GAB	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{\mathrm{GBA}}$
10	GND	20	V_{CC}

logic symbol† 'AS2620



logic symbol† AS2623



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† Pin numbers shown on logic symbols are for J and N packages only.

2640, 2645

OCTAL BUS TRANSCEIVERS/MOS DRIVERS

- Bidirectional octal bus transceivers for driving MOS devices
- I/O ports have 25 ohm series resistors so no external resistors are required
- Choice of true or inverting logic
- 3-state outputs

typical performance

TYPE	MAX SOURCE CURRENT	MAX SINK CURRENT
SN54AS2640	− 12 mA	48 mA
SN74AS2640	− 15 mA	64 mA
SN54AS2645	− 12 mA	48 mA
SN74AS2645	− 15 mA	64 mA

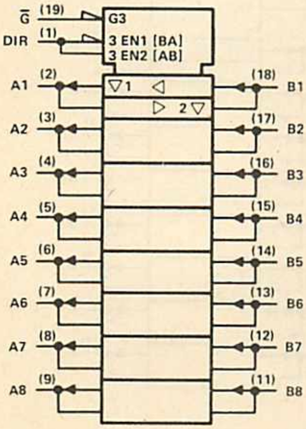
SN54AS2640 (J,FH) SN74AS2640 (N,FN)
SN54AS2645 (J,FH) SN74AS2645 (N,FN)

pin assignments

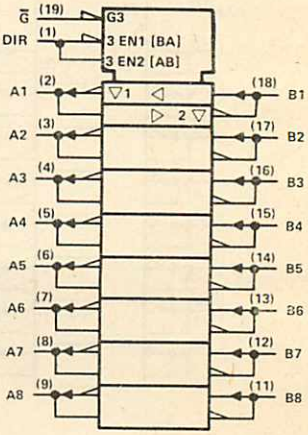
J,N PACKAGES			
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{G}$
10	GND	20	V_{CC}

FH,FN PACKAGES			
1	DIR	11	B8
2	A1	12	B7
3	A2	13	B6
4	A3	14	B5
5	A4	15	B4
6	A5	16	B3
7	A6	17	B2
8	A7	18	B1
9	A8	19	$\overline{G}$
10	GND	20	V_{CC}

logic symbol† 'AS2640



logic symbol† 'AS2645



† Pin numbers shown on logic symbols are for J and N packages only.

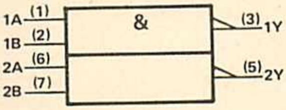
8003

DUAL 2-INPUT POSITIVE-NAND GATE

- Dual version of 'ALS00

SN54ALS8003 (JG,FH) SN74ALS8003 (P,FN)

logic symbol†



pin assignments

JG,P PACKAGE	
1	1A
2	1B
3	1Y
4	GND
5	2Y
6	2A
7	2B
8	V_{CC}

FH,FN PACKAGE			
1	nc	11	nc
2	1A	12	2Y
3	nc	13	nc
4	nc	14	nc
5	1B	15	2A
6	nc	16	nc
7	1Y	17	2B
8	nc	18	nc
9	nc	19	nc
10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for JG and P packages only.

'PAL16L8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

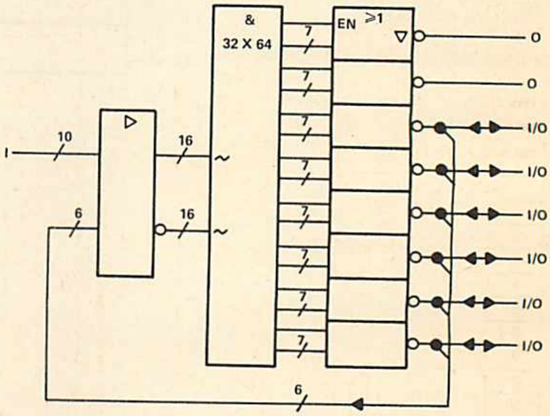
- Octal 16-input AND-OR-INVERT gate array

pin assignments

J, N PACKAGES			
1	I	11	I
2	I	12	O
3	I	13	I/O
4	I	14	I/O
5	I	15	I/O
6	I	16	I/O
7	I	17	I/O
8	I	18	I/O
9	I	19	O
10	GND	20	V_{CC}

SN54PAL16L8A (J) SN74PAL16L8A (J,N)

functional block diagram



~denotes fused inputs

'PAL16R4

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

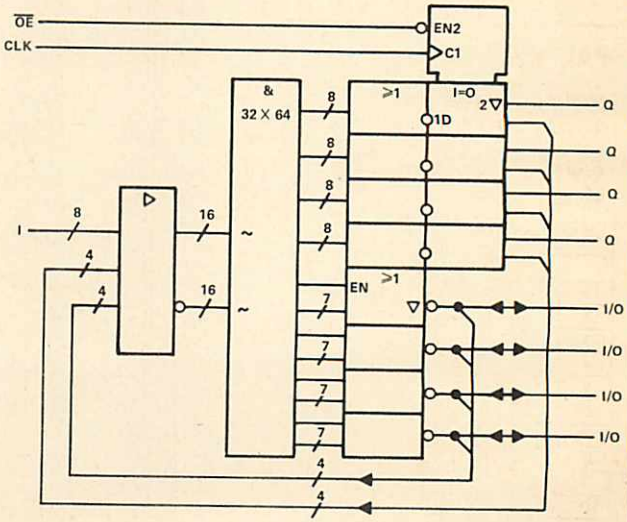
- Quad 16-input registered AND-OR gate array

pin assignments

J, N PACKAGES			
1	CLK	11	$\overline{OE}$
2	I	12	I/O
3	I	13	I/O
4	I	14	Q
5	I	15	Q
6	I	16	Q
7	I	17	Q
8	I	18	I/O
9	I	19	I/O
10	GND	20	V_{CC}

SN54PAL16R4A (J) SN74PAL16R4A (J,N)

functional block diagram



~denotes fused inputs

'PAL16R6

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

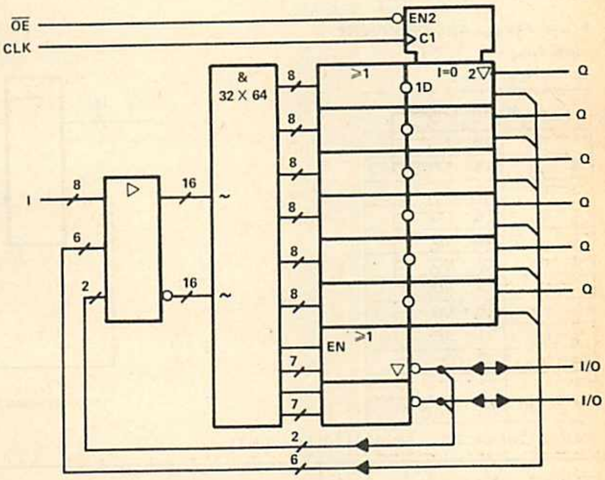
- Hex 16-input registered AND-OR gate array

pin assignments

J, N PACKAGES			
1	CLK	11	$\overline{OE}$
2	I	12	I/O
3	I	13	Q
4	I	14	Q
5	I	15	Q
6	I	16	Q
7	I	17	Q
8	I	18	Q
9	I	19	I/O
10	GND	20	V_{CC}

SN54PAL16R6A (J) SN74PAL16R6A (J,N)

functional block diagram



~denotes fused inputs

'PAL16R8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

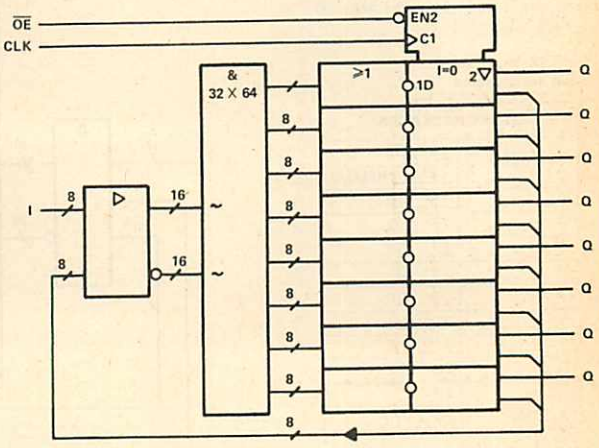
- Octal 16-input registered AND-OR gate array

pin assignments

J, N PACKAGES			
1	CLK	11	$\overline{OE}$
2	I	12	Q
3	I	13	Q
4	I	14	Q
5	I	15	Q
6	I	16	Q
7	I	17	Q
8	I	18	Q
9	I	19	Q
10	GND	20	V_{CC}

SN54PAL16R8A (J) SN74PAL16R8A (J,N)

functional block diagram



~denotes fused inputs

'PAL20L8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

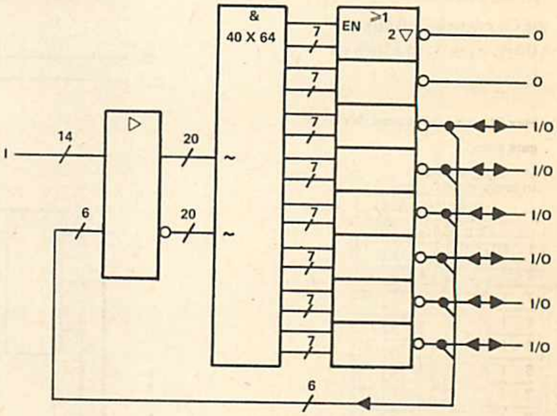
- Octal 20-input AND-OR-INVERT gate array

pin assignments

JT, NT PACKAGES			
1	I	13	I
2	I	14	I/PRELOAD
3	I	15	O
4	I	16	I/O
5	I	17	I/O
6	I	18	I/O
7	I	19	I/O
8	I	20	I/O
9	I	21	I/O
10	I	22	O
11	I	23	I
12	GND	24	V_{CC}

SN54PAL20L8A (JT) SN74PAL20L8A (JT,NT)

functional block diagram



~denotes fused inputs

'PAL20R4

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

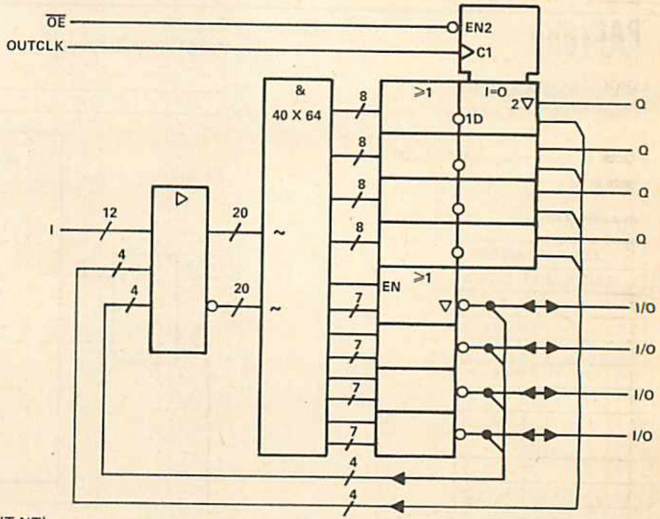
- Quad 20-input registered AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{OE}$
2	I	14	I/PRELOAD
3	I	15	I/O
4	I	16	I/O
5	I	17	Q
6	I	18	Q
7	I	19	Q
8	I	20	Q
9	I	21	I/O
10	I	22	I/O
11	I	23	I
12	GND	24	V_{CC}

SN54PAL20R4A (JT) SN74PAL20R4A (JT,NT)

functional block diagram



~denotes fused inputs

'PAL20R6

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

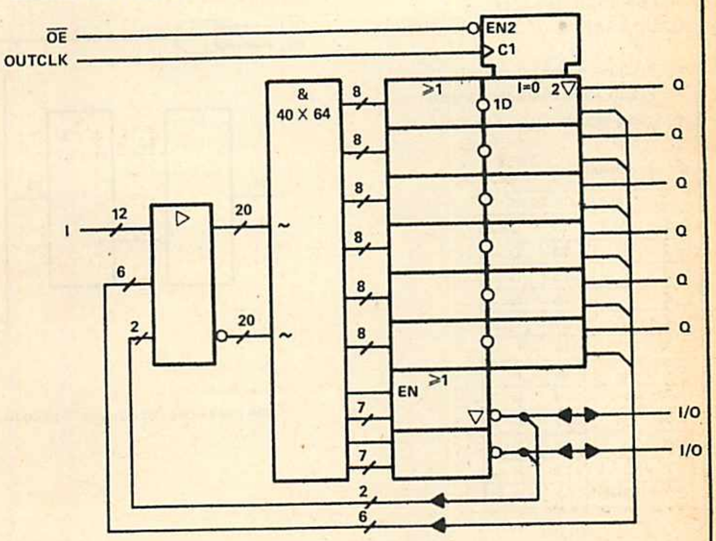
- Hex 20-input registered AND-OR gate array.

pin assignments

JT, NT PACKAGES	
1 OUT CLK	24 V_{CC}
2 I	23 I
3 I	22 I/O
4 I	21 Q
5 I	20 Q
6 I	19 Q
7 I	18 Q
8 I	17 Q
9 I	16 Q
10 I	15 I/O
11 I	14 I/PRELOAD
12 GND	13 $\overline{OE}$

SN54PAL20R6A (JT) SN74PAL20R6A (JT,NT)

functional block diagram



~ denotes fused inputs.

'PAL20R8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

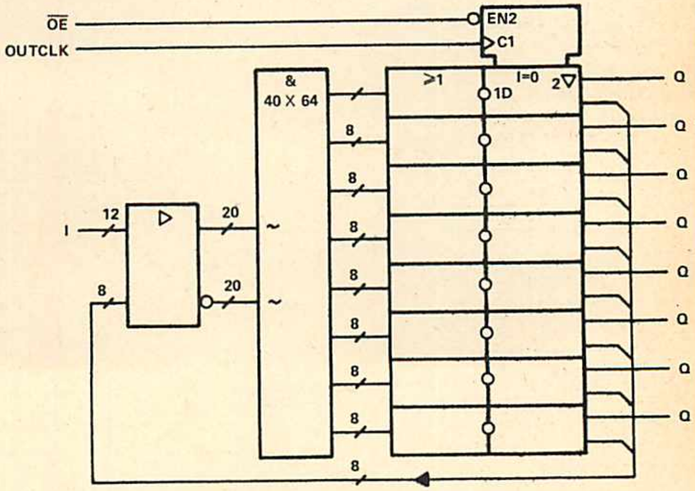
- Octal 20-input registered AND-OR gate array.

pin assignments

JT, NT PACKAGES	
1 OUT CLK	24 V_{CC}
2 I	23 I
3 I	22 Q
4 I	21 Q
5 I	20 Q
6 I	19 Q
7 I	18 Q
8 I	17 Q
9 I	16 Q
10 I	15 Q
11 I	14 I/PRELOAD
12 GND	13 $\overline{OE}$

SN54PAL20R8A (JT) SN74PAL20R8A (JT,NT)

functional block diagram



~ denotes fused inputs.

'PL839, PL840

FIELD-PROGRAMMABLE LOGIC ARRAYS

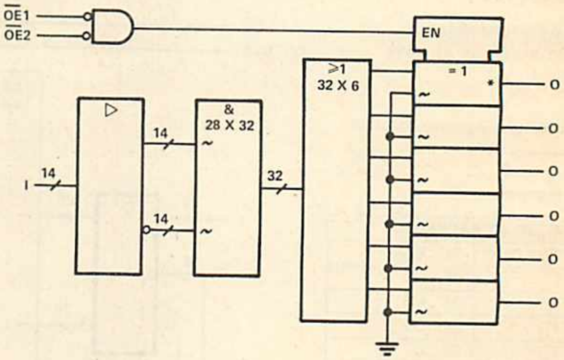
- 'PL839 – three-state outputs
- 'PL840 – open-collector outputs
- Programmable output polarity

pin assignments

J, JT, NT PACKAGES			
1	$\overline{\text{OE}}1$	13	$\overline{\text{OE}}2$
2	I	14	O
3	I	15	O
4	I	16	O
5	I	17	I
6	I	18	I
7	I	19	I
8	I	20	I
9	O	21	I
10	O	22	I
11	O	23	I
12	GND	24	V_{CC}

SN54PL839 (J)　SN74PL839 (JT,NT)
SN54PL840 (J)　SN74PL840 (JT,NT)

functional block diagram



~ denotes fused inputs.

* 'PL839 has 3-state (▽) outputs; 'PL840 has open-collector (♎) outputs.

nc – no internal connection.

'PALR19L8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

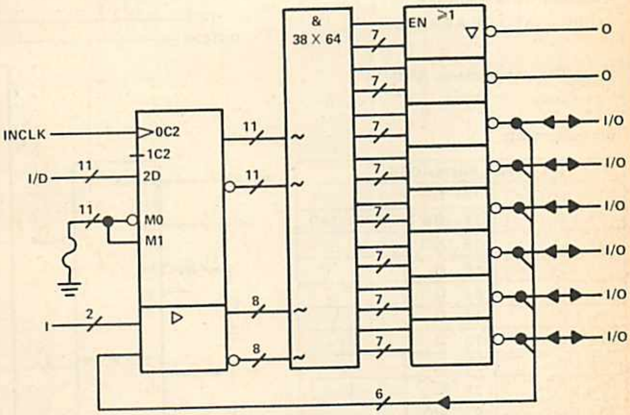
- Octal 19-input registered AND-OR-INVERT gate array

pin assignments

JT, NT PACKAGES			
1	I	13	I
2	I/D	14	INCLK/PRELOAD
3	I/D	15	O
4	I/D	16	I/O
5	I/D	17	I/O
6	I/D	18	I/O
7	I/D	19	I/O
8	I/D	20	I/O
9	I/D	21	I/O
10	I/D	22	O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PALR19L8 (JT) SN74PALR19L8 (JT,NT)

functional block diagram



'PALR19R4

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

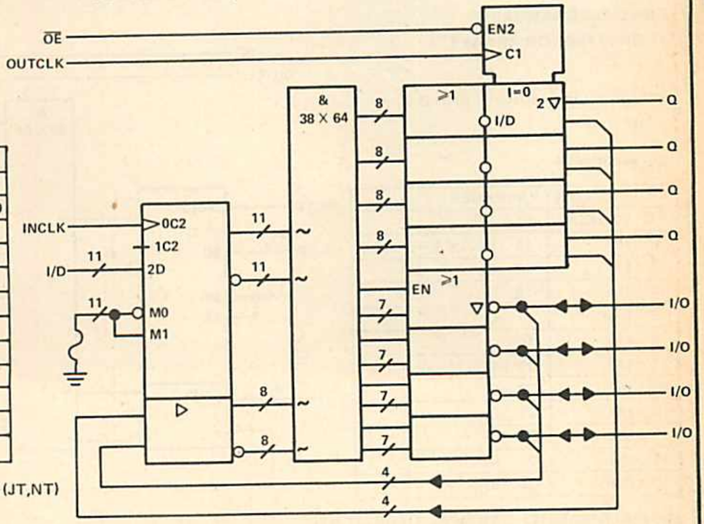
- Quad 19-input registered AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{OE}$
2	I/D	14	INCLK/PRELOAD
3	I/D	15	I/O
4	I/D	16	I/O
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	I/O
10	I/D	22	I/O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PALR19R4 (JT) SN74PALR19R4 (JT,NT)

functional block diagram



'PALR19R6

**FIELD-PROGRAMMABLE
LOGIC, FIXED-OR ARRAYS**

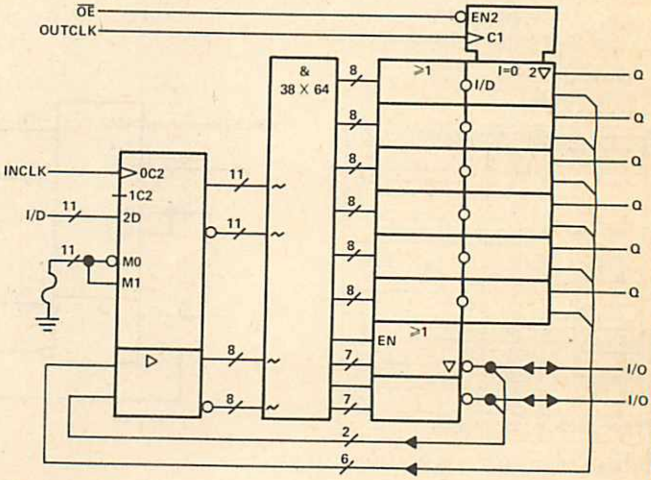
- Hex 19-input registered AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{\text{OE}}$
2	I/D	14	INCLK/PRELOAD
3	I/D	15	I/O
4	I/D	16	Q
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	Q
10	I/D	22	I/O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PALR19R6 (JT) SN74PALR19R6 (JT,NT)

functional block diagram



'PALR19R8

**FIELD-PROGRAMMABLE
LOGIC, FIXED-OR ARRAYS**

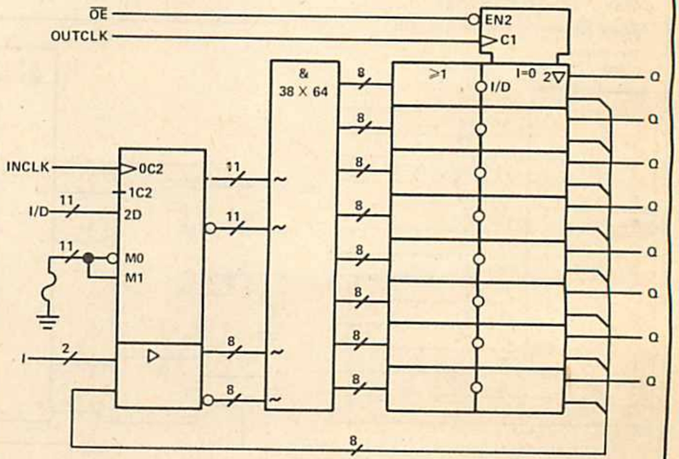
- Octal 19-input registered AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{\text{OE}}$
2	I/D	14	INCLK/PRELOAD
3	I/D	15	Q
4	I/D	16	Q
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	Q
10	I/D	22	Q
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PALR19R8 (JT) SN74PALR19R8 (JT,NT)

functional block diagram



'PALT19L8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

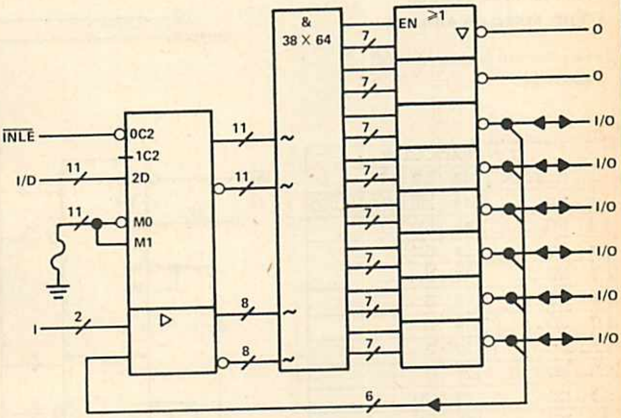
- Octal 19-input latched AND-OR-INVERT gate array

pin assignments

JT, NT PACKAGES			
1	I	13	I
2	I/D	14	$\overline{\text{INLE}}$/PRELOAD
3	I/D	15	O
4	I/D	16	I/O
5	I/D	17	I/O
6	I/D	18	I/O
7	I/D	19	I/O
8	I/D	20	I/O
9	I/D	21	I/O
10	I/D	22	O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PALT19L8 (JT) SN74PALT19L8 (JT,NT)

functional block diagram



'PALT19R4

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

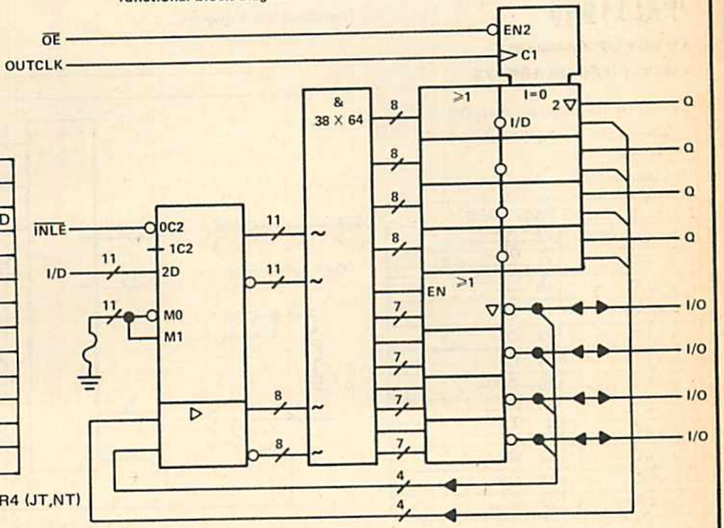
- Quad 19-input registered AND-OR gate array.

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{\text{OE}}$
2	I/D	14	$\overline{\text{INLE}}$/PRELOAD
3	I/D	15	I/O
4	I/D	16	I/O
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	I/O
10	I/D	22	I/O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PALT19R4 (JT) SN74PALT19R4 (JT,NT)

functional block diagram



'PALT19R6

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

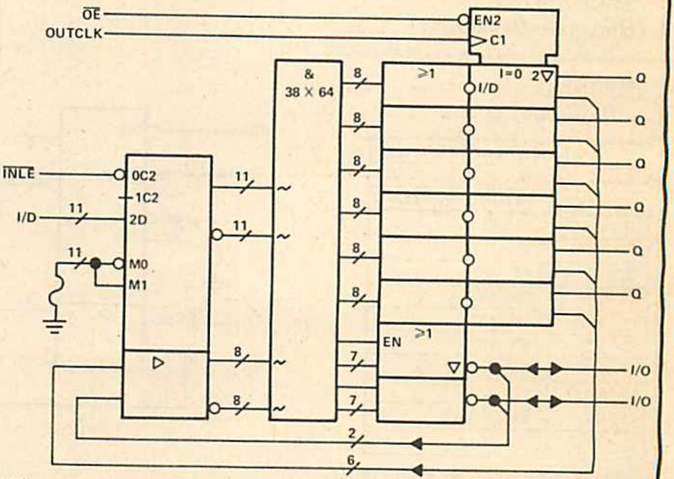
- Hex 19-input latched AND-OR gate array

pin assignments

JT, NT PACKAGES	
1 OUTCLK	13 $\overline{\text{OE}}$
2 I/D	14 $\overline{\text{INLE}}$/PRELOAD
3 I/D	15 I/O
4 I/D	16 Q
5 I/D	17 Q
6 I/D	18 Q
7 I/D	19 Q
8 I/D	20 Q
9 I/D	21 Q
10 I/D	22 I/O
11 I/D	23 I/D
12 GND	24 V_{CC}

SN54PALT19R6 (JT) SN74PALT19R6 (JT,NT)

functional block diagram



'PALT19R8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

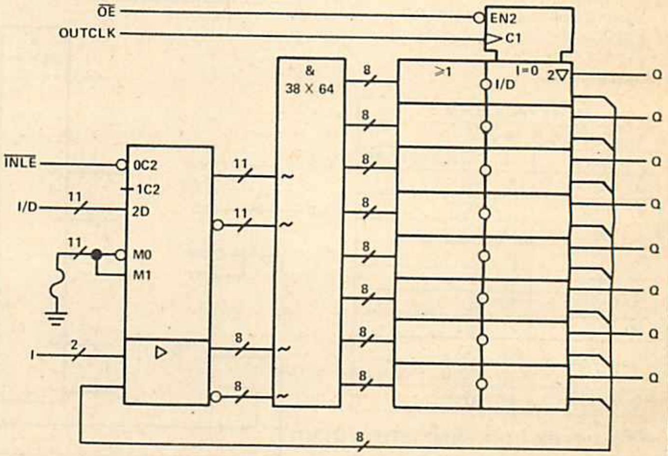
- Octal 19-input latched AND-OR gate array

pin assignments

JT, NT PACKAGES	
1 OUTCLK	13 $\overline{\text{OE}}$
2 I/D	14 $\overline{\text{INLE}}$/PRELOAD
3 I/D	15 Q
4 I/D	16 Q
5 I/D	17 Q
6 I/D	18 Q
7 I/D	19 Q
8 I/D	20 Q
9 I/D	21 Q
10 I/D	22 Q
11 I/D	23 I/D
12 GND	24 V_{CC}

SN54PALT19R8 (JT) SN74PALT19R8 (JT,NT)

functional block diagram



TBP14S10 ('S287) This product is no longer in production, it is replaced by TBP24S10.

TBP14SA10 ('S387) This product is no longer in production, it is replaced by TBP24SA10.

TBP18S22 ('S471) This product is no longer in production, it is replaced by TBP28L22.

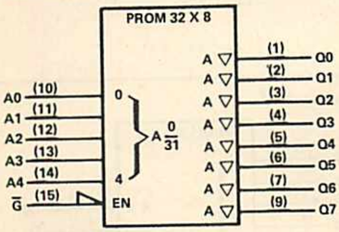
TBP18SA22 ('S470) This product is no longer in production, it is replaced by TBP28LA22.

TBP18S030 ('S288)

PROGRAMMABLE READ-ONLY MEMORIES

- 32 X 8
- Three-state outputs
- Typical address access time . . . 25 ns
- Typical power . . . 400 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 Q0	9 Q7
2 Q1	10 A0
3 Q2	11 A1
4 Q3	12 A2
5 Q4	13 A3
6 Q5	14 A4
7 Q6	15 G̅
8 GND	16 V_{CC}

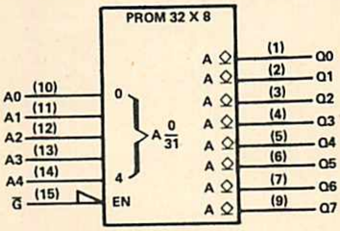
For chip carrier options and information, contact the factory.

TBP18SA030 ('S188)

PROGRAMMABLE READ-ONLY MEMORIES

- 32 X 8
- Open-collector outputs
- Typical address access time . . . 25 ns
- Typical power . . . 400 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 Q0	9 Q7
2 Q1	10 A0
3 Q2	11 A1
4 Q3	12 A2
5 Q4	13 A3
6 Q5	14 A4
7 Q6	15 G̅
8 GND	16 V_{CC}

For chip carrier options and information, contact the factory.

TBP18S42 ('S472) This product is no longer in production, it is replaced by TBP28S42.

TBP18SA42 ('S473) This product is no longer in production, it is replaced by TBP28SA42.

TBP18S46 ('S474) This product is no longer in production, it is replaced by TBP28S46.

TBP18SA46 ('S475) This product is no longer in production, it is replaced by TBP28SA46.

† Pin numbers shown on logic symbols are for J and N packages only.

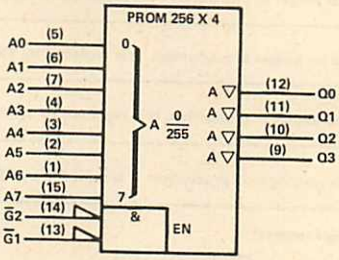
nc — no internal connection.

TBP24S10

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	9 Q3
2 A5	10 Q2
3 A4	11 Q1
4 A3	12 Q0
5 A0	13 G1
6 A1	14 G2
7 A2	15 A7
8 GND	16 V_{CC}

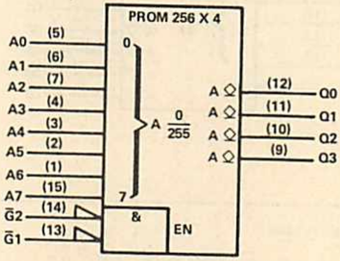
For chip carrier options and information, contact the factory.

TBP24SA10

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	9 Q3
2 A5	10 Q2
3 A4	11 Q1
4 A3	12 Q0
5 A0	13 G1
6 A1	14 G2
7 A2	15 A7
8 GND	16 V_{CC}

For chip carrier options and information, contact the factory.

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† Pin numbers shown on logic symbols are for J and N packages only.

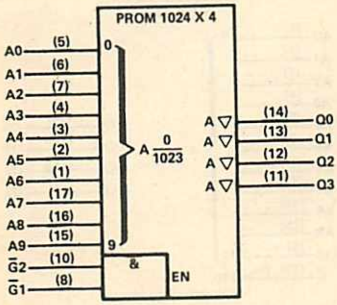
nc — no internal connection.

TBP24S41 ('S476)

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 4
- Three-state outputs
- Typical address access time . . . 40 ns
- Typical select time . . . 20 ns
- Typical power . . . 475 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	10 $\overline{G2}$
2 A5	11 Q3
3 A4	12 Q2
4 A3	13 Q1
5 A0	14 Q0
6 A1	15 A9
7 A2	16 A8
8 $\overline{G1}$	17 A7
9 GND	18 V_{CC}

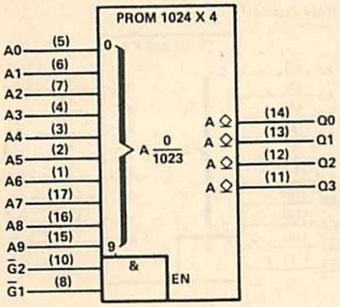
For chip carrier options and information, contact the factory.

TBP24SA41 ('S477)

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 4
- Open-collector outputs
- Typical address access time . . . 40 ns
- Typical select time . . . 20 ns
- Typical power . . . 475 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	10 $\overline{G2}$
2 A5	11 Q3
3 A4	12 Q2
4 A3	13 Q1
5 A0	14 Q0
6 A1	15 A9
7 A2	16 A8
8 $\overline{G1}$	17 A7
9 GND	18 V_{CC}

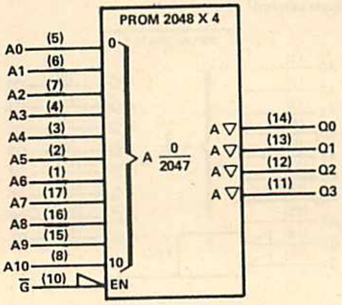
For chip carrier options and information, contact the factory.

TBP24S81 ('S454)

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 4
- Three-state outputs
- Typical address access time . . . 45 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	10 $\overline{G}$
2 A5	11 Q3
3 A4	12 Q2
4 A3	13 Q1
5 A0	14 Q0
6 A1	15 A9
7 A2	16 A8
8 A10	17 A7
9 GND	18 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.

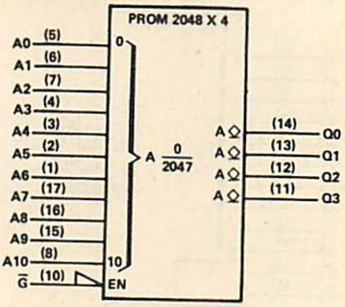
nc — no internal connection.

TBP24SA81 ('S455)

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 4
- Open-collector outputs
- Typical address access time . . . 45 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A6	10	$\overline{G}$
2	A5	11	Q3
3	A4	12	Q2
4	A3	13	Q1
5	A0	14	Q0
6	A1	15	A9
7	A2	16	A8
8	A10	17	A7
9	GND	18	V$_{CC}$

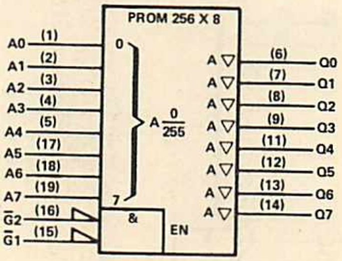
For chip carrier options and information, contact the factory.

TBP28L22

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Three-state outputs
- Typical address access time . . . 45 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	11	Q4
2	A1	12	Q5
3	A2	13	Q6
4	A3	14	Q7
5	A4	15	$\overline{G1}$
6	Q0	16	$\overline{G2}$
7	Q1	17	A5
8	Q2	18	A6
9	Q3	19	A7
10	GND	20	V$_{CC}$

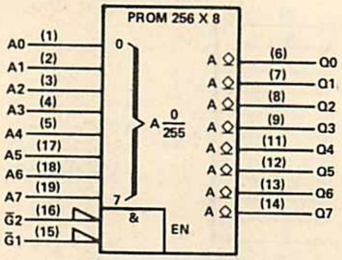
For chip carrier options and information, contact the factory.

TBP28LA22

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Open-collector outputs
- Typical address access time . . . 45 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	11	Q4
2	A1	12	Q5
3	A2	13	Q6
4	A3	14	Q7
5	A4	15	$\overline{G1}$
6	Q0	16	$\overline{G2}$
7	Q1	17	A5
8	Q2	18	A6
9	Q3	19	A7
10	GND	20	V$_{CC}$

For chip carrier options and information, contact the factory.

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† Pin numbers shown on logic symbols are for J and N packages only.

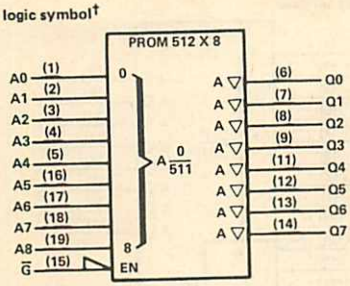
nc — no internal connection.

TBP28L42

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 55 ns
- Typical select time . . . 25 ns
- Typical power . . . 275 mW

logic symbol[†]



pin assignments

J, N PACKAGES			
1	A0	11	Q4
2	A1	12	Q5
3	A2	13	Q6
4	A3	14	Q7
5	A4	15	G̅
6	Q0	16	A5
7	Q1	17	A6
8	Q2	18	A7
9	Q3	19	A8
10	GND	20	V_{CC}

For chip carrier options and information, contact the factory.

[†] Pin numbers shown on logic symbols are for J and N packages only.

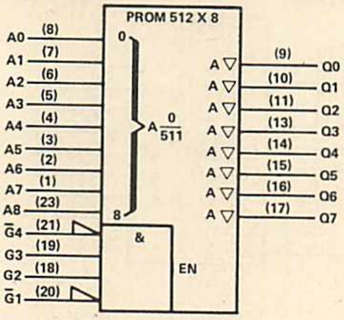
nc – no internal connection.

TBP28L45
TBP28L46

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 55 ns
- Typical select time . . . 25 ns
- Typical power . . . 275 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	G2
7	A1	19	G3
8	A0	20	$\overline{G}1$
9	Q0	21	$\overline{G}4$
10	Q1	22	nc
11	Q2	23	A8
12	GND	24	V_{CC}

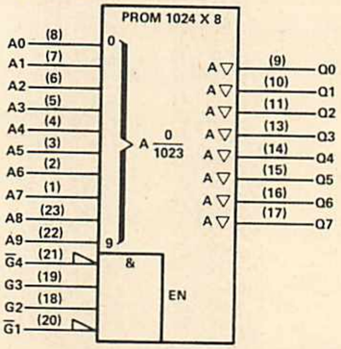
For chip carrier options and information, contact the factory.

TBP28L85A
TBP28L86A

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 65 ns
- Typical select time . . . 30 ns
- Typical power . . . 275 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	G2
7	A1	19	G3
8	A0	20	$\overline{G}1$
9	Q0	21	$\overline{G}4$
10	Q1	22	A9
11	Q2	23	A8
12	GND	24	V_{CC}

For chip carrier options and information, contact the factory.

TBP28L86 ('LS478)

This product is no longer in production, it is replaced by TBP28L86A.

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† Pin numbers shown on logic symbols are for J and N packages only.

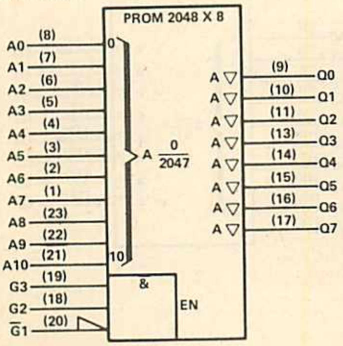
nc — no internal connection.

TBP28L165

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Three-state outputs
- Typical address access time . . . 65 ns
- Typical select time . . . 30 ns
- Typical power . . . 350 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}1$
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

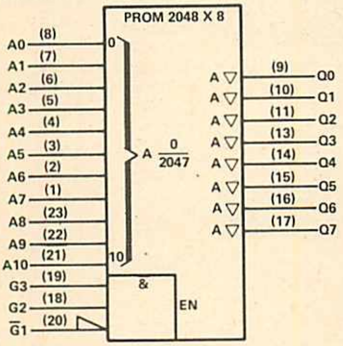
For chip carrier options and information, contact the factory.

TBP28L166

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Three-state outputs
- Typical address access time . . . 65 ns
- Typical select time . . . 30 ns
- Typical power . . . 350 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}1$
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

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† Pin numbers shown on logic symbols are for J and N packages only.

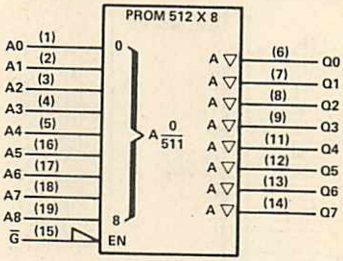
nc – no internal connection.

TBP28S42

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	11	Q4
2	A1	12	Q5
3	A2	13	Q6
4	A3	14	Q7
5	A4	15	G̅
6	Q0	16	A5
7	Q1	17	A6
8	Q2	18	A7
9	Q3	19	A8
10	GND	20	V_{CC}

For chip carrier options and information, contact the factory.

---

† Pin numbers shown on logic symbols are for J and N packages only.

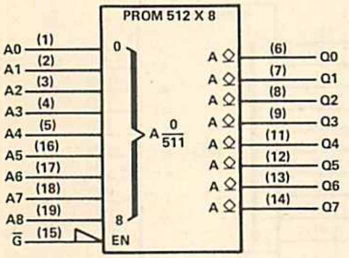
nc — no internal connection.

TBP28SA42

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	11	Q4
2	A1	12	Q5
3	A2	13	Q6
4	A3	14	Q7
5	A4	15	$\overline{G}$
6	Q0	16	A5
7	Q1	17	A6
8	Q2	18	A7
9	Q3	19	A8
10	GND	20	V_{CC}

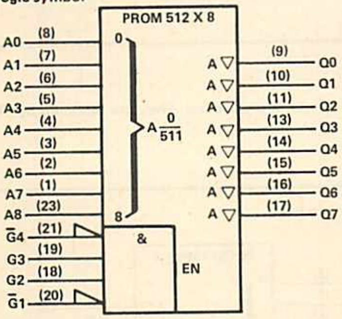
For chip carrier options and information, contact the factory.

TBP28S45
TBP28S46

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	G2
7	A1	19	G3
8	A0	20	$\overline{G1}$
9	Q0	21	$\overline{G4}$
10	Q1	22	nc
11	Q2	23	A8
12	GND	24	V_{CC}

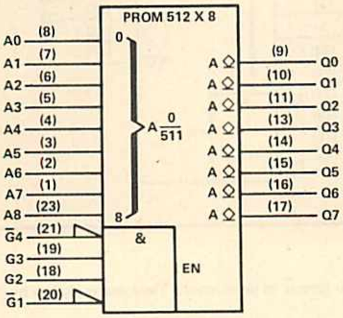
For chip carrier options and information, contact the factory.

TBP28SA46

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	G2
7	A1	19	G3
8	A0	20	$\overline{G1}$
9	Q0	21	$\overline{G4}$
10	Q1	22	nc
11	Q2	23	A8
12	GND	24	V_{CC}

For chip carrier options and information, contact the factory.

---

† Pin numbers shown on logic symbols are for J and N packages only.

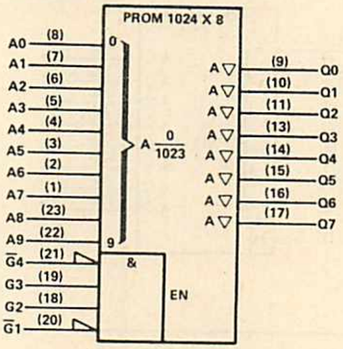
nc — no internal connection.

TBP28S85A

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	G2
7	A1	19	G3
8	A0	20	$\overline{\mathrm{G}}$1
9	Q0	21	$\overline{\mathrm{G}}$4
10	Q1	22	A9
11	Q2	23	A8
12	GND	24	V_{CC}

For chip carrier options and information, contact the factory.

TBP28S86 ('S478)
TBP28S86-60

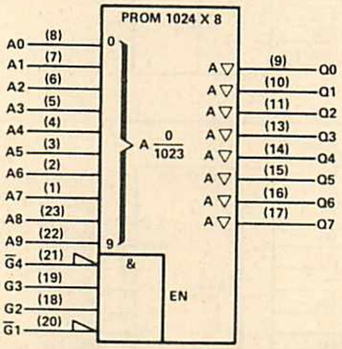
These products are no longer in production. They are replaced by TBP28S86A and TBP28S86A-50.

TBP28S86A

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 550 mw

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	G2
7	A1	19	G3
8	A0	20	$\overline{\mathrm{G}}$1
9	Q0	21	$\overline{\mathrm{G}}$4
10	Q1	22	A9
11	Q2	23	A8
12	GND	24	V_{CC}

For chip carrier options and information, contact the factory.

TBP28SA86 ('S479)
TBP28SA86-60

These products are no longer in production. They are replaced by TBP28SA86A

---

† Pin numbers shown on logic symbols are for J and N packages only.

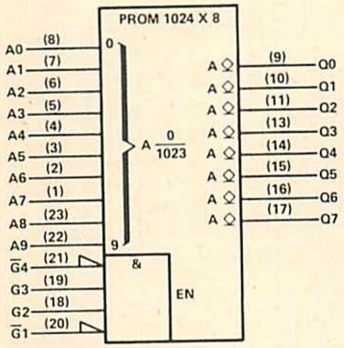
nc – no internal connection.

TBP28SA86A

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}1$
9 Q0	21 $\overline{G}4$
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

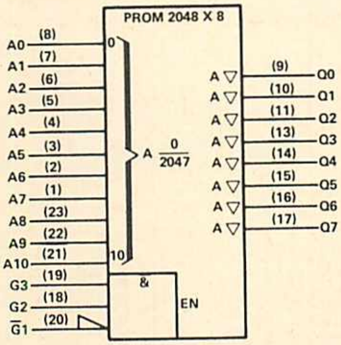
For chip carrier options and information, contact the factory.

TBP28S165
TBP28S166

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Three-state outputs
- Typical select time . . . 15 ns

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}1$
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

TYPE	PACKAGE ROW SPACING	TYPICAL ADDRESS ACCESS TIME	GUARANTEED MAXIMUM ACCESS TIME	TYPICAL POWER DISSIPATION
TBP28S165	7.62 mm (0.300 in.)	25 ns		550 mW
TBP28S166	15,24 mm (0.600 in.)	35 ns		650 mW

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† Pin numbers shown on logic symbols are for J and N packages only.

nc – no internal connection.

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If you have questions on this Explanation
of New Logic Symbols, Please contact:

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IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC)
publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

EXPLANATION OF NEW LOGIC SYMBOLS

by F. A. Mann

1 INTRODUCTION

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in Section 4.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

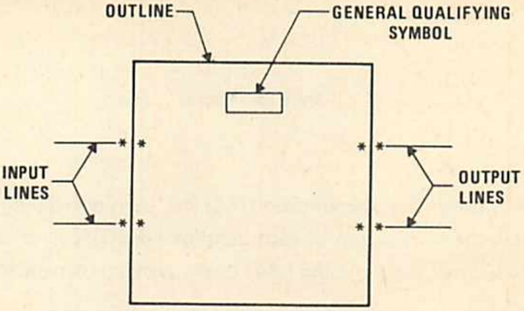
Internationally, Working Group 2 of IEC Technical Committee TC-3 is preparing a new document (Publication 617-12) that will consolidate the original work started in the mid 1960's and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 is revising the publication IEEE Std 91/ANSI Y32.14. Texas Instruments is participating in the work of both organizations and this Data Book introduces new logic symbols in anticipation of the new standards. When changes are made as the standards develop, future editions will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications will finally contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this book; comparing the symbols with functional block diagrams and/or function tables will further help that understanding.

2 SYMBOL COMPOSITION

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbols is not significant. As shown in Figure 1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table I shows the general qualifying symbols used in this data book. Input lines are placed on the left and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 11.

All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated qualifying symbol or label inside the element.



*Possible positions for qualifying symbols relating to inputs and outputs

FIGURE 1 – SYMBOL COMPOSITION

The outlines of elements may be abutted or embedded in which case the following conventions apply. There is no logic connection between the elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection between the elements when the line common to their outlines is perpendicular to the direction of signal flow. The number of logic connections between elements will be clarified by the use of qualifying symbols and this is discussed further under that topic. If no indications are shown on either side of the common line, it is assumed there is only one connection.

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2 shows that unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

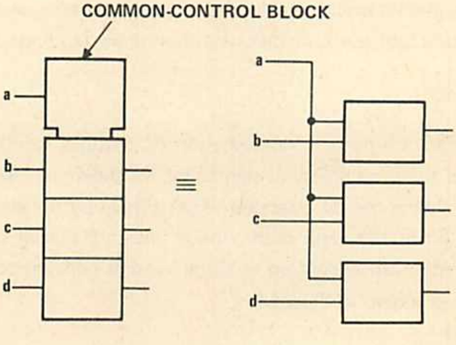


FIGURE 2 – ILLUSTRATION OF COMMON- CONTROL BLOCK

A common output depending on all elements of the array can be shown as the output of a common-output element. Its distinctive visual feature is the double line at its top. In addition the common-output element may have other inputs as shown in Figure 3. The function of the common-output element must be shown by use of a general qualifying symbol.

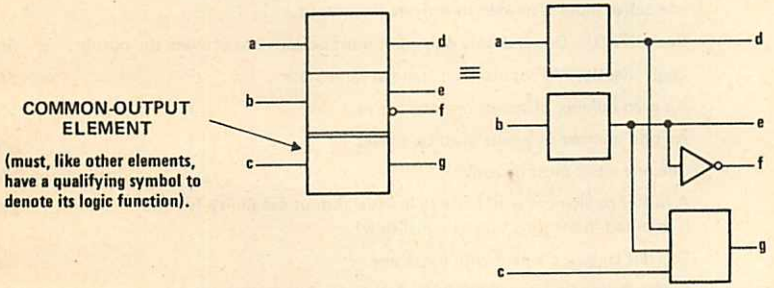

COMMON-OUTPUT ELEMENT
(must, like other elements, have a qualifying symbol to denote its logic function).
a
b
c
d
e
f
g
≡
a
b
c
d
e
f
g

FIGURE 3 – ILLUSTRATION OF COMMON-OUTPUT ELEMENT

3 QUALIFYING SYMBOLS

3.1 General Qualifying Symbols

Table I shows the general qualifying symbols used in this data book. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

3.2 Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table II and will be familiar to most users with the possible exception of the logic polarity and analog signal indicators. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in this data book in the symbology for actual devices. The presence of the triangular polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

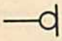
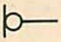
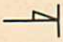
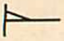
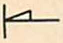
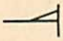
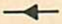
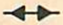
EXPLANATION OF NEW LOGIC SYMBOLS

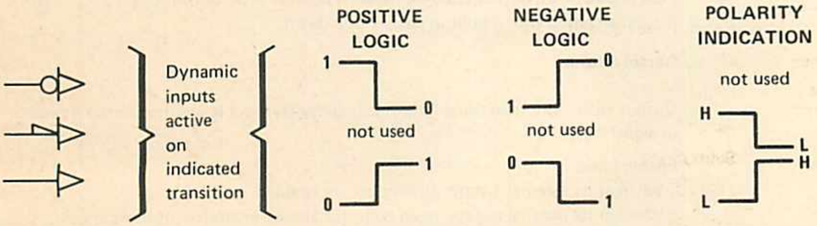
TABLE I – GENERAL QUALIFYING SYMBOLS

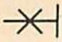
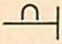
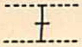
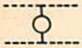
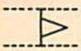
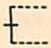
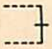
SYMBOL	DESCRIPTION	EXAMPLE
&	AND gate or function.	SN7400
>1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.	SN7402
=1	Exclusive OR. One and only one input must be active to activate the output.	SN7486
=	Logic identity. All inputs must stand at same state.	SN74180
2k	An even number of inputs must be active.	SN74180
2k+1	An odd number of inputs must be active.	SN74ALS86
1	The one input must be active.	SN7404
▷ or ◁	A buffer or element with more than usual output capability (symbol is oriented in the direction of signal flow).	SN74S436
⎎	Schmitt trigger; element with hysteresis.	SN74LS18
X/Y	Coder, code converter (DEC/BCD, BIN/OUT, BIN/7-SEG, etc.).	SN74LS347
MUX	Multiplexer/data selector.	SN74150
DMUX or DX	Demultiplexer.	SN74138
Σ	Adder.	SN74LS385
P–Q	Subtracter.	SN74LS385
CPG	Look-ahead carry generator.	SN74182
π	Multiplier.	SN74LS384
COMP	Magnitude comparator.	SN74LS682
ALU	Arithmetic logic unit.	SN74LS381
⎍	Retriggerable monostable.	SN74LS422
1⎍	Non-retriggerable monostable (one-shot).	SN74121
G ⎍⎍	Astable element. Showing waveform is optional.	SN74LS320
!G ⎍⎍	Synchronously starting astable.	SN74LS624
G! ⎍⎍	Astable element that stops with a completed pulse.	*
SRGm	Shift register. m = number of bits.	SN74LS595
CTRm	Counter. m = number of bits; cycle length = 2^m.	SN54LS590
CTR DIVm	Counter with cycle length = m.	SN74LS668
RCTRm	Asynchronous (ripple-carry) counter; cycle length = 2^m.	*
ROM	Read-only memory.	SN74187
RAM	Random-access read/write memory.	SN74170
FIFO	First-in, first-out memory.	SN74LS222
I=0	Element powers up cleared to 0 state.	SN74AS877
Φ	Highly complex function; "gray box" symbol with limited detail shown under special rules.	SN74LS608

*Not all of the general qualifying symbols have been used in this book, but they are included here for the sake of completeness.

TABLE II – QUALIFYING SYMBOLS FOR INPUTS AND OUTPUTS

	Logic negation at input. External 0 produces internal 1.
	Logic negation at output. Internal 1 produces external 0.
	Active-low input. Equivalent to in positive logic.
	Active-low output. Equivalent to in positive logic.
	Active-low input in the case of right-to-left signal flow.
	Active-low output in the case of right-to-left signal flow.
	Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.
	Bidirectional signal flow.



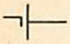
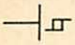
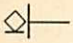
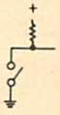
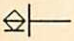
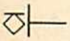
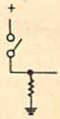
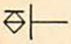
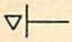
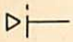
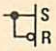
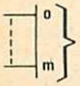
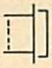
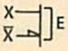
	Nonlogic connection. A label inside the symbol will usually define the nature of this pin.
	Input for analog signals.
	Internal connection. 1 state on left produces 1 state on right.
	Negated internal connection. 1 state on left produces 0 state on right.
	Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.
	Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship.
	Internal output (virtual output). Its effect on an internal input to which it is connected is indicated by dependency notation.

The internal connections between logic elements abutted together in a symbol may be indicated by the symbols shown. Each logic connection may be shown by the presence of qualifying symbols at one or both sides of the common line and if confusion can arise about the numbers of connections, use can be made of one of the internal connection symbols.

The internal (virtual) input is an input originating somewhere else in the circuit and is not connected directly to a terminal. The internal (virtual) output is likewise not connected directly to a terminal.

EXPLANATION OF NEW LOGIC SYMBOLS

TABLE III – SYMBOLS INSIDE THE OUTLINE

	Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level. See § 5.
	Bi-threshold input (input with hysteresis)
	NPN open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection. 
	Passive-pull-up output is similar to NPN open-collector output but is suplemented with a built-in passive pull-up.
	NPN open-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection. 
	Passive-pull-down output is similar to NPN open-emitter output but is supplemented with a built-in passive pull-down.
	3-state output
	Output with more than usual output capability (symbol is oriented in the direction of signal flow).
EN	Enable input When at its internal 1-state, all outputs are enabled. When at its internal 0-state, open-collector and open-emitter outputs are off, three-state outputs are at normally defined internal logic states and at external high-impedance state, and all other outputs (e.g., totem-poles) are at the internal 0-state.
J, K, R, S, T	Usual meanings associated with flip-flops (e.g., R = reset, T = toggle)
D	Data input to a storage element equivalent to: 
→m ←m	Shift right (left) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
+m −m	Counting up (down) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
	Binary grouping. m is highest power of 2.
CT = 15	The contents-setting input, when active, causes the content of a register to take on the indicated value.
CT = 9	The content output is active if the content of the register is as indicated.
	Input line grouping . . . . indicates two or more terminals used to implement a single logic input. e.g., The paired expander inputs of SN7450. 
"1"	Fixed-state output always stands at its internal 1 state. For example, see SN74185.

The application of internal inputs and outputs requires an understanding of dependency notation, which is explained in Section 4.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN54LS440 symbol illustrates this principle.

3.3 Symbols Inside the Outline

Table III shows some symbols used inside the outline. Note particularly that open-collector, open-emitter, and three-state outputs have distinctive symbols. Also note that an EN input affects all of the outputs of the circuit and has no effect on inputs. When an enable input affects only certain outputs and/or affects one or more inputs, a form of dependency notation will indicate this (see 4.9). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in Section 8. Binary-weighted inputs are arranged in order and the binary weights of the least-significant and the most-significant lines are indicated by numbers. In this data book weights of input and output lines will be represented by powers of two usually only when the binary grouping symbol is used, otherwise, decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation. See Figure 28. A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Other symbols are used inside the outlines in this data book in accordance with the IEC/IEEE standards but are not shown here. Generally these are associated with arithmetic operations and are self-explanatory.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these].

4 DEPENDENCY NOTATION

4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful, symbols possible. It provides the means of denoting the *relationship* between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected". In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, ten types of dependency have been defined and all of these are used in this data book. They are listed below in the order in which they are presented and are summarized in Table IV following 4.11.

Section	Dependency Type or Other Subject
4.2	G, AND
4.3	General rules for dependency notation
4.4	V, OR
4.5	N, Negate, (Exclusive OR)
4.6	Z, Interconnection
4.7	C, Control
4.8	S, Set and R, Reset
4.9	EN, Enable
4.10	M, Mode
4.11	A, Address

4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While nine other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

In Figure 4 input **b** is ANDed with input **a** and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

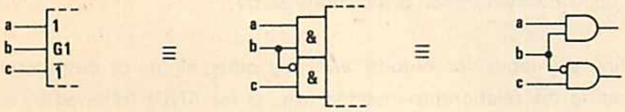


FIGURE 4 – G DEPENDENCY BETWEEN INPUTS

In Figure 5, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 6 shows input **a** to be ANDed with a dynamic input **b**.

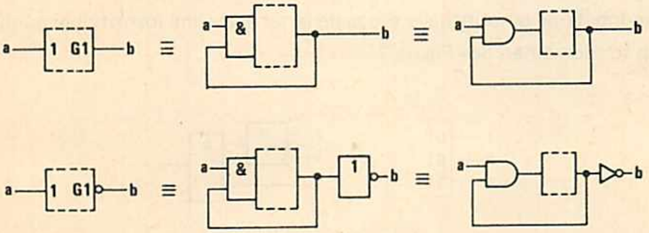


FIGURE 5 – G DEPENDENCY BETWEEN OUTPUTS AND INPUTS

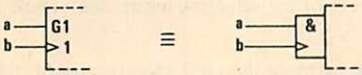


FIGURE 6 – G DEPENDENCY WITH A DYNAMIC INPUT

The rules for G dependency can be summarized thus:

When a G*m* input or output (*m* is a number) stands at its internal 1 state, all inputs and outputs affected by G*m* stand at their normally defined internal logic states. When the G*m* input or output stands at its 0 state, all inputs and outputs affected by G*m* stand at their internal 0 states.

4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

1) labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen, and
2) labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs. See Figure 4.

If two affecting inputs or outputs have the same letter and same identifying number, they stand in an OR relationship to each other. See Figure 7.

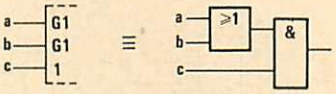


FIGURE 7 – OR'ED AFFECTING INPUTS

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input. See Figure 12.

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships. See Figure 12.

If the labels denoting the functions of affected inputs or outputs must be numbers, (e.g., outputs of a coder), the identifying numbers to be associated with both affecting inputs and affected inputs or outputs will be replaced by another character selected to avoid ambiguity, e.g., Greek letters. See Figure 8.

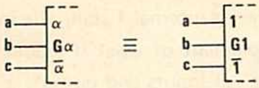


FIGURE 8 – SUBSTITUTION FOR NUMBERS

4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V. See Figure 9.

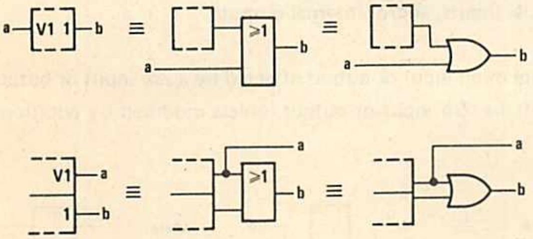
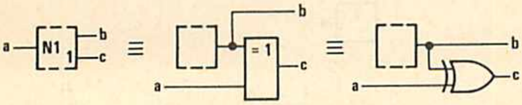


FIGURE 9 – V (OR) DEPENDENCY

When a V*m* input or output stands at its internal 1 state, all inputs and outputs affected by V*m* stand at their internal 1 states. When the V*m* input or output stands at its internal 0 state, all inputs and outputs affected by V*m* stand at their normally defined internal logic states.

4.5 N (Negate) (X-OR) Dependency

The symbol denoting negate dependency is the letter N. See Figure 10. Each input or output affected by an N*m* input or output stands in an exclusive-OR relationship with the N*m* input or output.



If a = 0, then c = b
If a = 1, then c = $\overline{b}$

FIGURE 10 – N (NEGATE) (X-OR) DEPENDENCY

When an N*m* input or output stands at its internal 1 state, the internal logic state of each input and each output affected by N*m* is the complement of what it would otherwise be. When an N*m* input or output stands at its internal 0 state, all inputs and outputs affected by N*m* stand at their normally defined internal logic states.

4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Z*m* input or output will be the same as the internal logic state of the Z*m* input or output, unless modified by additional dependency notation. See Figure 11.

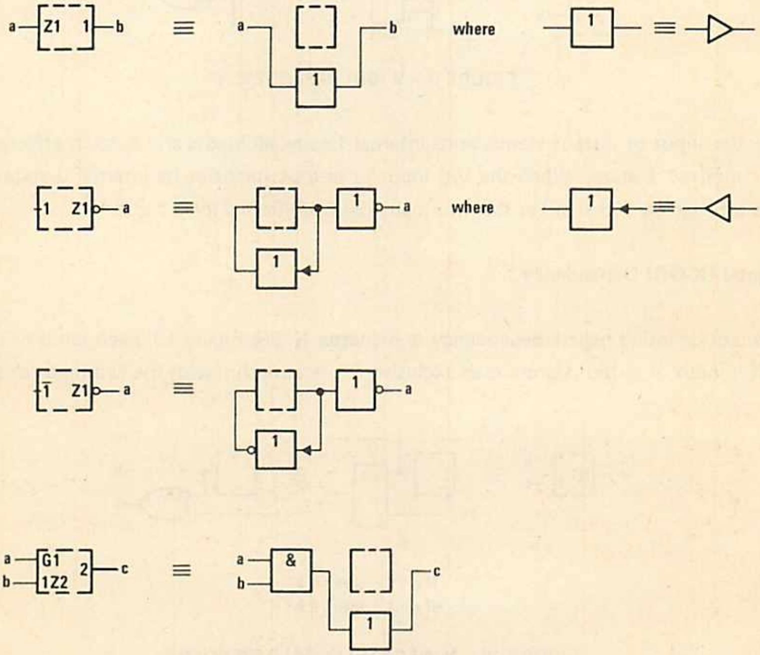
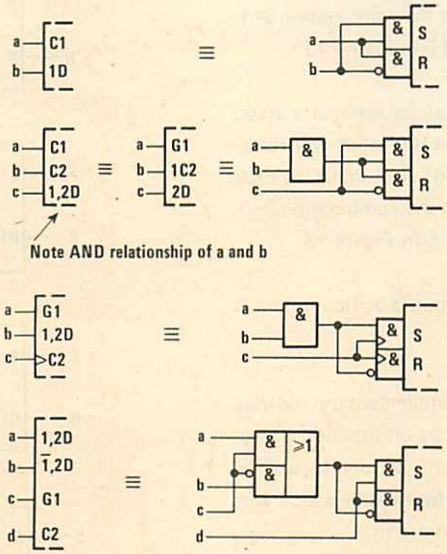


FIGURE 11 – Z (INTERCONNECTION) DEPENDENCY

4.7 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case the dynamic input symbol is used as shown in the third example of Figure 12.



Note AND relationship of a and b

Input c selects which of a or b is stored when d goes low.

FIGURE 12 – C (CONTROL) DEPENDENCY

When a C*m* input or output stands at its internal 1 state, the inputs affected by C*m* have their normally defined effect on the function of the element, i.e., these inputs are enabled. When a C*m* input or output stands at its internal 0 state, the inputs affected by C*m* are disabled and have no effect on the function of the element.

4.8 S (Set) and R (Reset) Dependencies

The symbol denoting set dependency is the letter S. The symbol denoting reset dependency is the letter R.

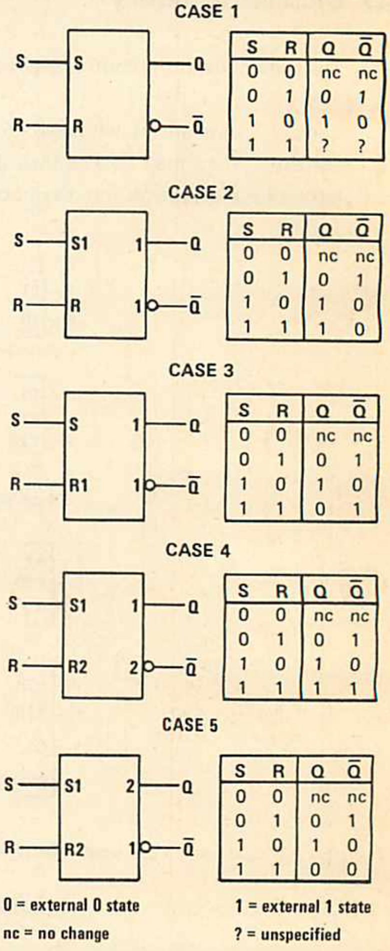
Set and reset dependencies are used if it is necessary to specify the effect of the combination R=S=1 on a bistable element. Case 1 in Figure 13 does not use S or R dependency.

When an S*m* input is at its internal 1 state, outputs affected by the Sm input will react, regardless of the state of an R input, as they normally would react to the combination S=1, R=0. See cases 2, 4, and 5 in Figure 13.

When an R*m* input is at its internal 1 state, outputs affected by the Rm input will react, regardless of the state of an S input, as they normally would react to the combination S=0, R=1. See cases 3, 4, and 5 in Figure 13.

When an S*m* or R*m* input is at its internal 0 state, it has no effect.

Note that the noncomplementary output patterns in cases 4 and 5 are only pseudo stable. The simultaneous return of the inputs to S=R=0 produces an unforeseeable stable and complementary output pattern.



CASE 1

S	R	Q	$\overline{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	?	?

CASE 2

S	R	Q	$\overline{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	0

CASE 3

S	R	Q	$\overline{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	1

CASE 4

S	R	Q	$\overline{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	1

CASE 5

S	R	Q	$\overline{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	0

0 = external 0 state
1 = external 1 state
nc = no change
? = unspecified

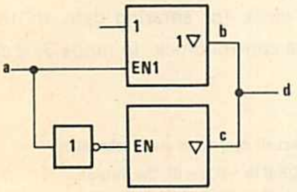
FIGURE 13 – S (SET) AND R (RESET) DEPENDENCIES

4.9 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An EN*m* input has the same effect on outputs as an EN input, see 3.1, but it effects only those outputs labeled with the identifying number *m*. It also affects those inputs labeled with the identifying number *m*. By contrast, an EN input affects all outputs and no inputs. The effect of an EN*m* input on an affected input is identical to that of a C*m* input. See Figure 14.

When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element and the outputs affected by this input stand at their normally defined internal logic states, i.e., these inputs and outputs are enabled.



If a = 0, b is disabled and d = c
If a = 1, c is disabled and d = b

FIGURE 14 – EN (ENABLE) DEPENDENCY

When an EN*m* input stands at its internal 0 state, the inputs affected by EN*m* are disabled and have no effect on the function of the element, and the outputs affected by EN*m* are also disabled. Open-collector outputs are turned off, three-state outputs stand at their normally defined internal logic states but externally exhibit high impedance, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

4.10 M (Mode) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting M*m* inputs will appear in the label of that affected input or output between parentheses and separated by solidi. See Figure 19.

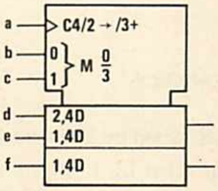
4.10.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an M*m* input or M*m* output stands at its internal 1 state, the inputs affected by this M*m* input or M*m* output have their normally defined effect on the function of the element, i.e., the inputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, the inputs affected by this M*m* input or M*m* output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the M*m* input or M*m* output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

EXPLANATION OF NEW LOGIC SYMBOLS

The circuit in Figure 15 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d**, **e**, and **f** are D inputs subject to dynamic control *(clocking) by the* **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading) and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

FIGURE 15 – M (MODE) DEPENDENCY AFFECTING INPUTS

4.10.2 M Dependency Affecting Outputs

When an M*m* input or M*m* output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states, i.e., the outputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that M*m* input or M*m* output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this M*m* input or M*m* output appears are to be ignored.

In Figure 16, mode 1 exists when the **a** input stands at its internal 1 state. The delayed output symbol is effective only in mode 1 (when input **a** = 1) in which case the device functions as a pulse-triggered flip-flop. See Section 5. When input **a** = 0, the device is not in mode 1 so the delayed output symbol has no effect and the device functions as a transparent latch.

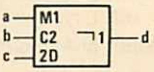


FIGURE 16 – TYPE OF FLIP-FLOP DETERMINED BY MODE

In Figure 17, if input a stands at its internal 1 state establishing mode 1, output b will stand at its internal 1 state only when the content of the register equals 9. Since output **b** is located in the common-control block with no defined function outside of mode 1, the state of this output outside of mode 1 is not defined by the symbol.

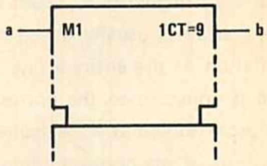


FIGURE 17 – DISABLING AN OUTPUT OF THE COMMON-CONTROL BLOCK

In Figure 18, if input a stands at its internal 1 state establishing mode 1, output b will stand at its internal 1 state only when the content of the register equals 15. If input a stands at its internal 0 state, output b will stand at its internal 1 state only when the content of the register equals 0.

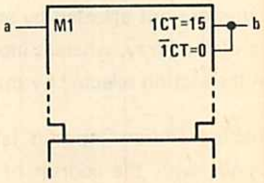


FIGURE 18 – DETERMINING AN OUTPUT'S FUNCTION

In Figure 19 inputs a and b are binary weighted to generate the numbers 0, 1, 2, or 3. This determines which one of the four modes exists.

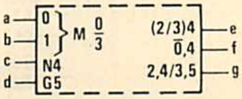


FIGURE 19 – DEPENDENT RELATIONSHIPS AFFECTED BY MODE

At output **e** the label set causing negation (if **c** = 1) is effective only in modes 2 and 3. In modes 0 and 1 this output stands at its normally defined state as if it had no labels. At output **f** the label set has effect when the mode is not 0 so output **e** is negated (if **c** = 1) in modes 1, 2, and 3. In mode 0 the label set has no effect so the output stands at its normally defined state. In this example 0,4 is equivalent to (1/2/3)4. At output **g** there are two label sets. The first set, causing negation (if **c** = 1), is effective only in mode 2. The second set, subjecting **g** to AND dependency on **d**, has effect only in mode 3.

Note that in mode 0 none of the dependency relationships has any effect on the outputs, so **e**, **f**, and **g** will all stand at the same state.

4.11 A (Address) Dependency

The symbol denoting address dependency is the letter A.

Address dependency provides a clear representation of those elements, particularly memories, that use address control inputs to select specified sections of a multidimensional array. Such a section of a memory array is usually called a word. The purpose of address dependency is to allow a symbolic presentation of the entire array. An input of the array shown at a particular element of this general section is common to the corresponding elements of all selected sections of the array. An output of the array shown at a particular element of this general section is the result of the OR function of the outputs of the corresponding elements of selected sections. If the label of an output of the array shown at a particular element of this general section indicates that this output is an open-circuit output or a three-state output, then this indication refers to the output of the array and not to those of the sections of the array.

Inputs that are not affected by any affecting address input have their normally defined effect on all sections of the array, whereas inputs affected by an address input have their normally defined effect only on the section selected by that address input.

An affecting address input is labelled with the letter A followed by an identifying number that corresponds with the address of the particular section of the array selected by this input. Within the general section presented by the symbol, inputs and outputs affected by an A*m* input are labelled with the letter A, which stands for the identifying numbers, i.e., the addresses, of the particular sections.

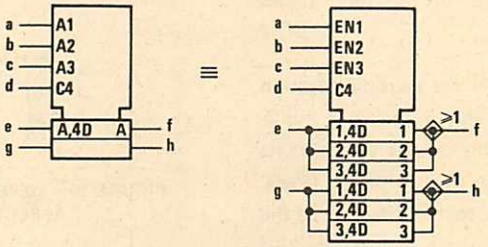


FIGURE 20 – A (ADDRESS) DEPENDENCY

Figure 20 shows a 3-word by 2-bit memory having a separate address line for each word and uses EN dependency to explain the operation. To select word 1, input a is taken to its 1 state, which establishes mode 1. Data can now be clocked into the inputs marked "1,4D". Unless words 2 and 3 are also selected, data cannot be clocked in at the inputs marked "2,4D" and "3,4D". The outputs will be the OR functions of the selected outputs, i.e., only those enabled by the active EN functions.

The identifying numbers of affecting address inputs correspond with the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency-inputs (e.g., G, V, N, . . .), because in the general section presented by the symbol they are replaced by the letter A.

If there are several sets of affecting *Am* inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter A is modified to 1A, 2A, . . . Because they have access to the same sections of the array, these sets of A inputs may have the same identifying numbers.

Figure 21 is another illustration of the concept.

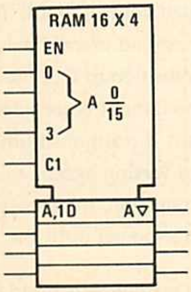


FIGURE 21

FIGURE 21 – ARRAY OF 16 SECTIONS OF FOUR TRANSPARENT LATCHES WITH 3-STATE OUTPUTS COMPRISING A 16-WORD X 4-BIT RANDOM-ACCESS MEMORY

TABLE IV – SUMMARY OF DEPENDENCY NOTATION

TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs. ◇outputs off. ▽outputs at external high impedance, no change in internal logic state. Other outputs at internal 0 state.
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (X-OR)	N	Complements state	No effect
RESET	R	Affected output reacts as it would to S = 0, R = 1	No effect
SET	S	Affected output reacts as it would to S = 1, R = 0	No effect
OR	V	Imposes 1 state	Permits action
Interconnection	Z	Imposes 1 state	Imposes 0 state

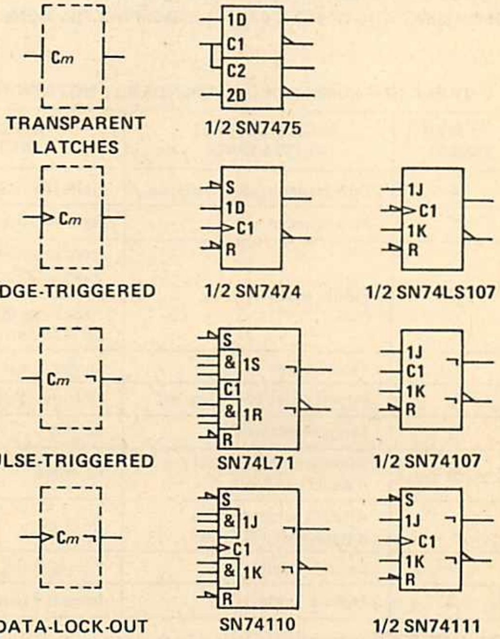
*These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described under "Symbols Inside The Outline", see 3.1.

5 BISTABLE ELEMENTS

The dynamic input symbol, the postponed output symbol, and dependency notation provide the tools to differentiate four main types of bistable elements and make synchronous and asynchronous inputs easily recognizable. See Figure 22. The first column shows the essential distinguishing features; the other columns show examples.

Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C. Pulse-triggered elements require the setup of data before the start of the control pulse; the C input is considered static since the data must be maintained as long as C is at its 1 state. The output is postponed until C returns to its 0 state. The data-lock-out element is similar to the pulse-triggered version except that the C input is considered dynamic in that shortly after C goes through its active transition, the data inputs are disabled and data does not have to be held. However, the output is still postponed until the C input returns to its initial external level.

Notice that synchronous inputs can be readily recognized by their dependency labels (1D, 1J, 1K, 1S, 1R) compared to the asynchronous inputs (S, R), which are not dependent on the C inputs.



TRANSPARENT LATCHES — 1/2 SN7475

EDGE-TRIGGERED — 1/2 SN7474 — 1/2 SN74LS107

PULSE-TRIGGERED — SN74L71 — 1/2 SN74107

DATA-LOCK-OUT — SN74110 — 1/2 SN74111

FIGURE 22 – FOUR TYPES OF BISTABLE CIRCUITS

6 CODERS

The general symbol for a coder or code converter is shown in Figure 23. X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and at the outputs, respectively.

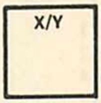


FIGURE 23 – CODER GENERAL SYMBOL

Indication of code conversion is based on the following rule:

> Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

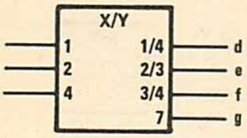
The indication of the relationships between the internal logic states of the inputs and the internal value is accomplished by:

1) labelling the inputs with numbers. In this case the internal value equals the sum of the weights associated with those inputs that stand at their internal 1-state, or by
2) replacing X by an appropriate indication of the input code and labelling the inputs with characters that refer to this code.

The relationships between the internal value and the internal logic states of the outputs are indicated by:

1) labelling each output with a list of numbers representing those internal values that lead to the internal 1-state of that output. These numbers shall be separated by solidi as in Figure 24. This labelling may also be applied when Y is replaced by a letter denoting a type of dependency (see Section 7). If a continuous range of internal values produces the internal 1 state of an output, this can be indicated by two numbers that are inclusively the beginning and the end of the range, with these two numbers separated by three dots, e.g., 4 . . . 9 = 4/5/6/7/8/9, or by
2) replacing Y by an appropriate indication of the output code and labelling the outputs with characters that refer to this code as in Figure 25.

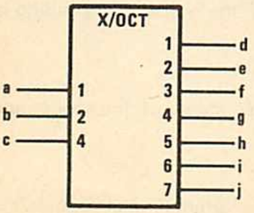
Alternatively, the general symbol may be used together with an appropriate reference to a table in which the relationship between the inputs and outputs is indicated. This is a recommended way to symbolize a PROM after it has been programmed.



TRUTH TABLE

INPUTS			OUTPUTS			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

FIGURE 24 – AN X/Y CODE CONVERTER



TRUTH TABLE

INPUTS			OUTPUTS							
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

FIGURE 25 – AN X/OCTAL CODE CONVERTER

7 USE OF A CODER TO PRODUCE AFFECTING INPUTS

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case use can be made of the symbol for a coder as an embedded symbol. See Figure 26.

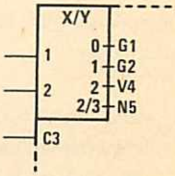


FIGURE 26 – PRODUCING VARIOUS TYPES OF DEPENDENCIES

If all affecting inputs produced by a coder are of the same type and their identifying numbers correspond with the numbers shown at the outputs of the coder, Y (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. The indications of the affecting inputs should then be omitted. See Figure 27.

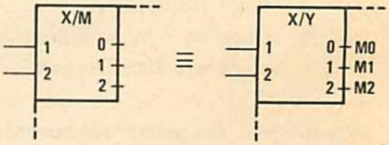


FIGURE 27 – PRODUCING ONE TYPE OF DEPENDENCY

8 USE OF BINARY GROUPING TO PRODUCE AFFECTING INPUTS

If all affecting inputs produced by a coder are of the same type and have consecutive identifying numbers not necessarily corresponding with the numbers that would have been shown at the outputs of the coder, use can be made of the binary grouping symbol (see 3.1). k external lines effectively generate 2^k internal inputs. The bracket is followed by the letter denoting the type of dependency followed by $\frac{m1}{m2}$. The m1 is to be replaced by the smallest identifying number and the m2 by the largest one, as shown in Figure 28.

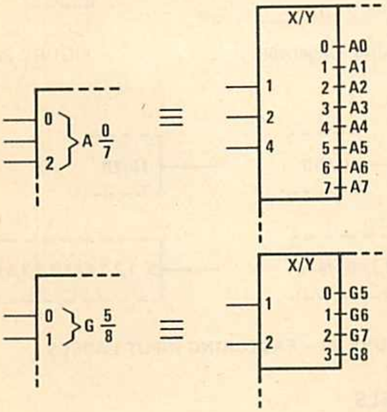


FIGURE 28 – USE OF THE BINARY GROUPING SYMBOL

9 SEQUENCE OF INPUT LABELS

If an input having a single functional effect is affected by other inputs, the qualifying symbol (if there is any) for that functional effect is preceded by the labels corresponding to the affecting inputs. The left-to-right order of these preceding labels is the order in which the effects or modifications must be applied. The affected input has no functional effect on the element if the logic state of any one of the affecting inputs, considered separately, would cause the affected input to have no effect, regardless of the logic states of other affecting inputs.

If an input has several different functional effects or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of presentation is not advantageous. In those cases the input may be shown once with the different sets of labels separated by solidi. See Figure 29. No meaning is attached to the order of these sets of labels. If one of the functional effects of an input is that of an unlabelled input of the element, a solidus will precede the first set of labels shown.

If all inputs of a combinational element are disabled (caused to have no effect on the function of the element), the internal logic states of the outputs of the element are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed and the outputs remain at their existing internal logic states.

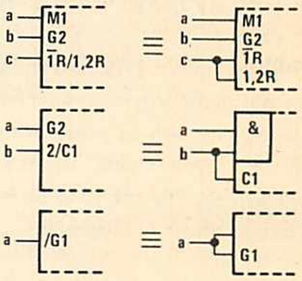


FIGURE 29 – INPUT LABELS

Labels may be factored using algebraic techniques.

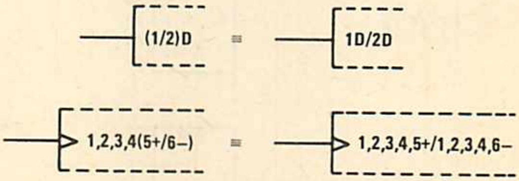


FIGURE 30 – FACTORING INPUT LABELS

10 SEQUENCE OF OUTPUT LABELS

If an output has a number of different labels, regardless of whether they are identifying numbers of affecting inputs or outputs or not, these labels are shown in the following order:

1) if the postponed output symbol has to be shown, this comes first, if necessary preceded by the indications of the inputs to which it must be applied;

2) followed by the labels indicating modifications of the internal logic state of the output, such that the left-to-right order of these labels corresponds with the order in which their effects must be applied;

3) followed by the label indicating the effect of the output on inputs and other outputs of the element.

Symbols for open-circuit or three-state outputs, where applicable, are placed just inside the outside boundary of the symbol adjacent to the output line. See Figure 31.

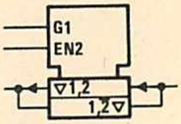


FIGURE 31 – PLACEMENT OF 3-STATE SYMBOLS

If an output needs several different sets of labels that represent alternative functions (e.g., depending on the mode of action), these sets may be shown on different output lines that must be connected outside the outline. However, there are cases in which this method of presentation is not advantageous. In those cases the output may be shown once with the different sets of labels separated by solidi. See Figure 32.

Two adjacent identifying numbers of affecting inputs in a set of labels that are not already separated by a nonnumeric character should be separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting M*m* input standing at its internal 0 state, this set of labels has no effect on that output.

Labels may be factored using algebraic techniques.

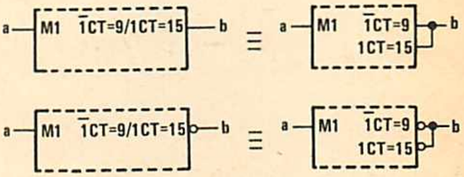


FIGURE 32 – OUTPUT LABELS

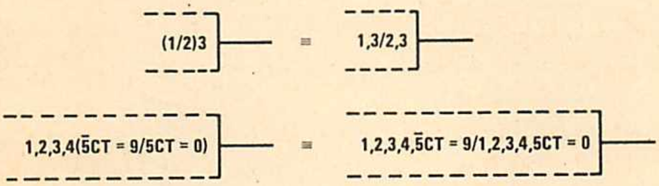

(1/2)3
≡
1,3/2,3
1,2,3,4($\overline{5}$CT = 9/5CT = 0)
≡
1,2,3,4,$\overline{5}$CT = 9/1,2,3,4,5CT = 0

FIGURE 33 – FACTORING OUTPUT LABELS

If you have questions on this Explanation of New Logic Symbols, please contact:

F.A. Mann MS 49
Texas Instruments Incorporated
P.O. Box 225012
Dallas, Texas 75265
Telephone (214) 995-2867

IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

The TTL Data Book
Volume 1

General Information 1

Functional Index 2

Product Guide 3

Logic Symbols 4

Mechanical Data 5

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: SN 54ALS01 J -00

1. Prefix

MUST CONTAIN TWO TO FOUR LETTERS

SN	Standard Prefix
SNJ	MIL-STD-883 Processed
JANB	MIL-M-38510 Processed

2. Unique Circuit Description

MUST CONTAIN SIX TO TWELVE CHARACTERS

Examples:

54ALS00A
74AS74
74ALS1645A
74ALS1645A-1

3. Package

MUST CONTAIN ONE OR TWO LETTERS

J, JD, JT, JW, N, NT, NW (Dual-in-line packages)[†]

FH, FK, FE or FN (Chip carriers)

(From pin-connection diagram on individual data sheet)

4. Instructions (Dash No.)

MUST CONTAIN TWO NUMBERS

- 00 No special instructions
- 10 Solder-dipped leads (N and NT packages only)

[†] These circuits in dual-in-line packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs.

Dual-in-line (J, JD, JT, JW, N, NT, NW)

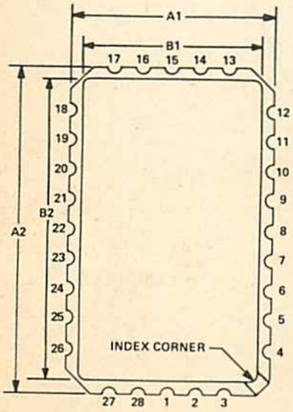
- Slide Magazines
- A-Channel Plastic Tubing
- Barnes Carrier (N only)
- Sectioned Cardboard Box
- Individual Plastic Box

FE ceramic chip carrier packages

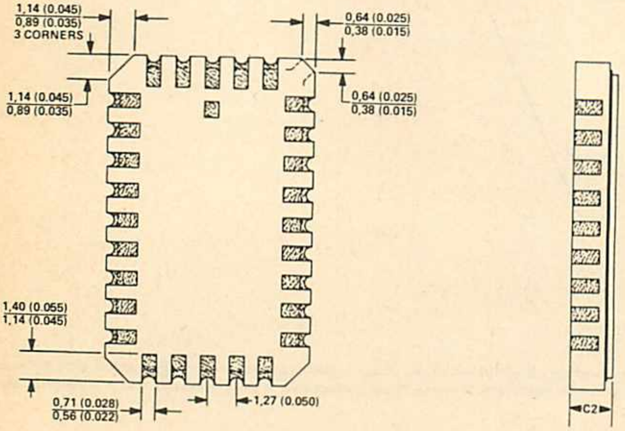
Each of these hermetically sealed leadless chip carrier packages has a metal cap, a 3-layer ceramic base, and a brazed seal. The packages are intended for surface mounting on solder lands on 1,27-mm (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

RECTANGULAR FE CERAMIC CHIP CARRIER PACKAGE

(28-terminal package shown)



NUMBER OF TERMINALS	A1		A2		B1		B2		C2	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
28	8,76 (0.345)	9,02 (0.355)	13,84 (0.545)	14,10 (0.555)	7,80 (0.307)	7.95 (0.313)	12,88 (0.507)	13,03 (0.513)	1,65 (0.065)	2,01 (0.079)
32	11,30 (0.445)	11,56 (0.455)	13,84 (0.545)	14,10 (0.555)	10,34 (0.407)	13,03 (0.513)	12,88 (0.507)	13,03 (0.513)	1,65 (0.065)	2,01 (0.079)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

FH and FK ceramic chip carrier packages

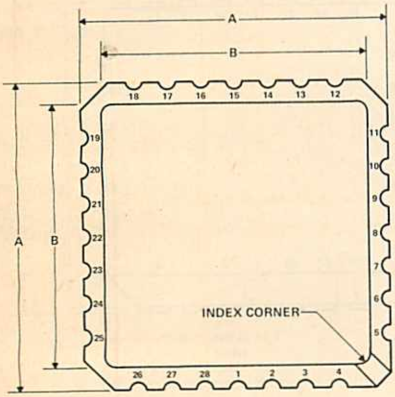
Both versions of these hermetically sealed chip carrier packages have ceramic bases. The FH package has a single-layer base with a ceramic lid and glass seal. The FK package has a three-layer base with a metal lid and braze seal.

The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FH and FK packages are identical to the FC and FD packages, respectively. The new designations are used to indicate devices whose terminal assignments conform to a forthcoming JEDEC Standard.

FH AND FK CERAMIC CHIP CARRIER PACKAGES

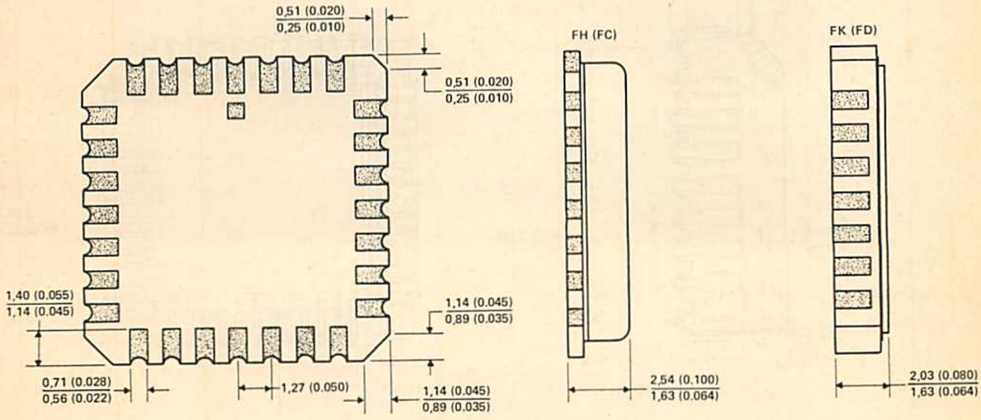
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.422)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)
MS004CD	44	16,26 (0.640)	16,76 (0.660)	12,58 (0.495)	14,22 (0.560)
MS004CE	52	18,78 (0.739)	19,32 (0.761)	12,58 (0.495)	14,22 (0.560)
MS004CF	68	23,83 (0.938)	24,43 (0.962)	12,6 (0.495)	21,8 (0.862)
MS004CG	84	28,83 (1.135)	29,59 (1.165)	12,6 (0.495)	27,0 (1.065)

*All dimensions and notes for the specified JEDEC outline apply.



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

MECHANICAL DATA

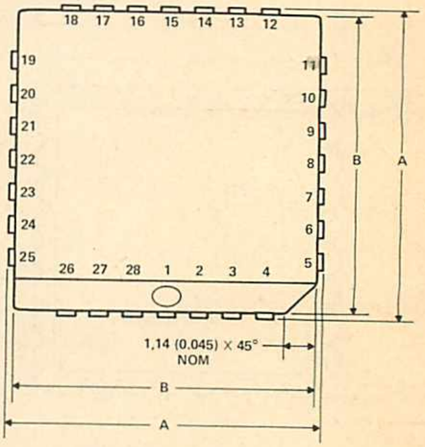
FN plastic chip carrier package

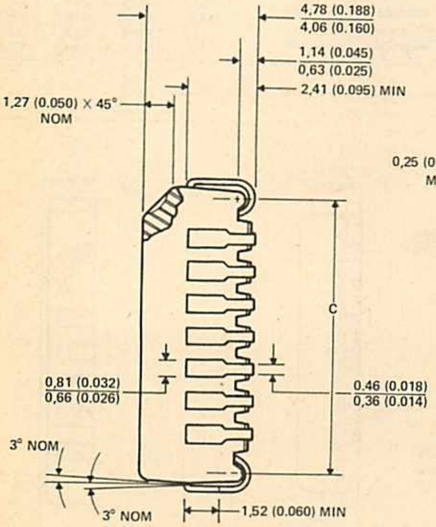
Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27-mm (0.050-inch) centers. Leads require no additional cleaning or processing when used in soldered assembly.

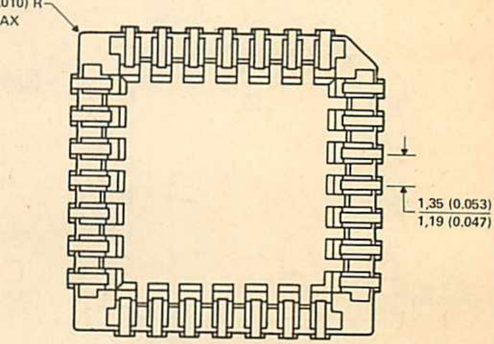
FN PLASTIC CHIP CARRIER PACKAGE

(28-terminal package shown)

NO. OF TERMINALS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
20	9,70 (0.382)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	8,08 (0.318)	8,38 (0.330)
28	12,24 (0.482)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,62 (0.418)	10,92 (0.430)
44	17,32 (0.682)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,70 (0.618)	16,00 (0.630)
52	19,86 (0.782)	20.19 (0.795)	19,05 (0.750)	19,20 (0.756)	18,24 (0.718)	18,54 (0.730)
68	24,94 (0.982)	25,27 (0.995)	24.13 (0.950)	24,28 (0.956)	23,32 (0.918)	23,62 (0.930)



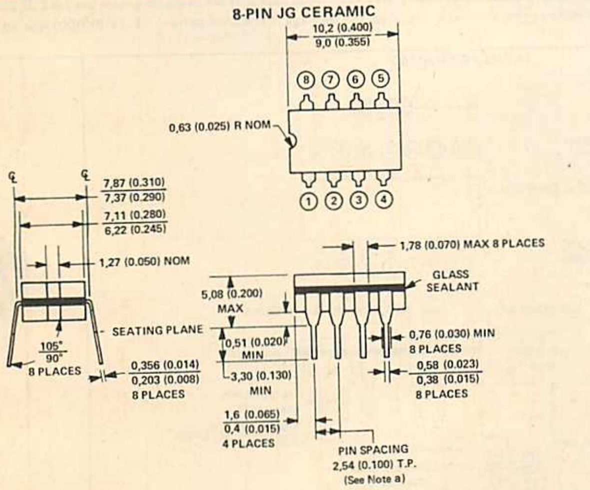




ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

JG ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and 8-lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Non-shiny tin-plated leads require no additional cleaning or processing when used in soldered assembly.



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

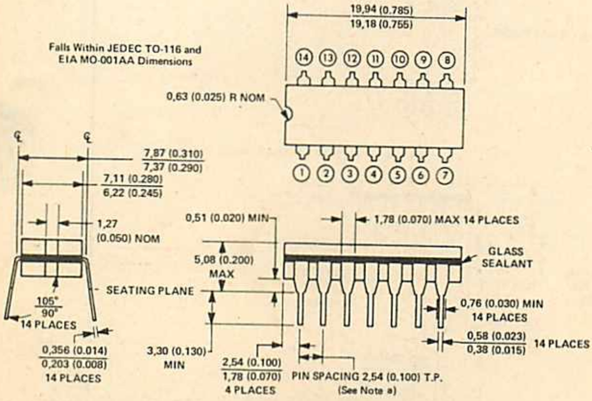
MECHANICAL DATA

J ceramic packages (including JT and JW dual-in-line and JQ quad-in-line packages)

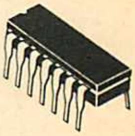
Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The JT packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers, JW packages for mounting-hole rows on 15,24 (0.600) centers, and the JQ quad-in-line package for mounting-hole rows on 15,24 (0.600) and 20,32 (0.800) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing. For the 24-pin packages, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.

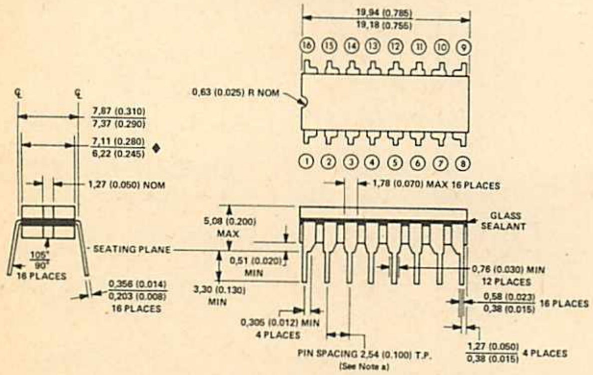
14-PIN J CERAMIC


Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions
19,94 (0.785) / 19,18 (0.755)
⑭ ⑬ ⑫ ⑪ ⑩ ⑨ ⑧
0,63 (0.025) R NOM
① ② ③ ④ ⑤ ⑥ ⑦
℄ ℄
7,87 (0.310) / 7,37 (0.290)
7,11 (0.280) / 6,22 (0.245)
1,27 (0.050) NOM
0,51 (0.020) MIN
1,78 (0.070) MAX 14 PLACES
GLASS SEALANT
5,08 (0.200) MAX
SEATING PLANE
105° / 90° 14 PLACES
0,76 (0.030) MIN 14 PLACES
0,58 (0.023) / 0,38 (0.015) 14 PLACES
0,356 (0.014) / 0,203 (0.008) 14 PLACES
3,30 (0.130) MIN
2,54 (0.100) / 1,78 (0.070) 4 PLACES
PIN SPACING 2,54 (0.100) T.P. (See Note a)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

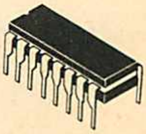


16-PIN J CERAMIC



◆For memories of 64 bits and up and a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, this maximum is 7,62 (0.300). All other dimensions apply without modification.

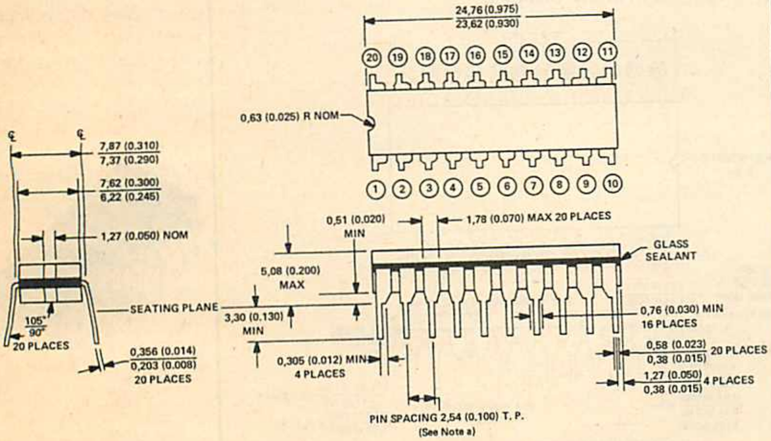
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.



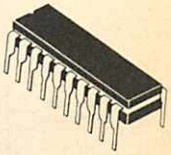
NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J ceramic dual-in-line packages (continued)

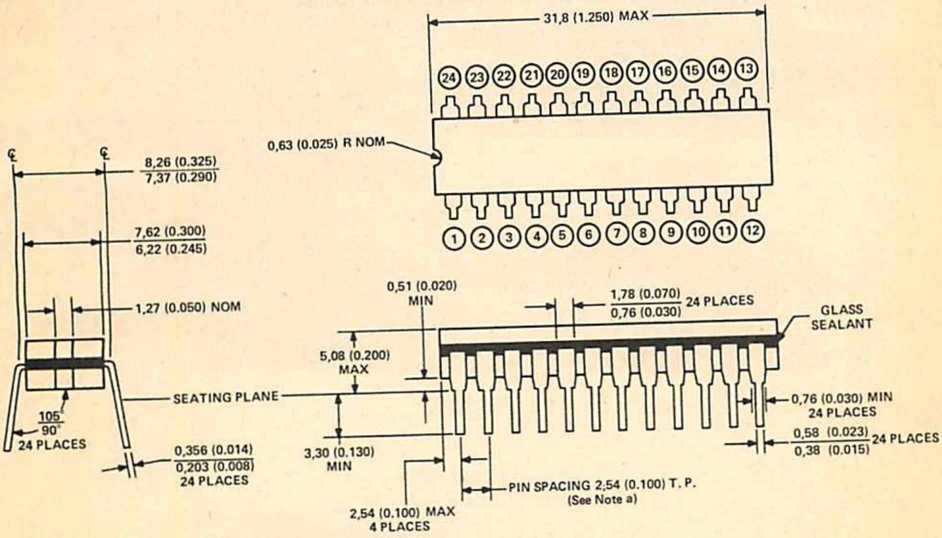
20-PIN J CERAMIC



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.



24-PIN JT CERAMIC, 0.300-INCH ROW SPACING

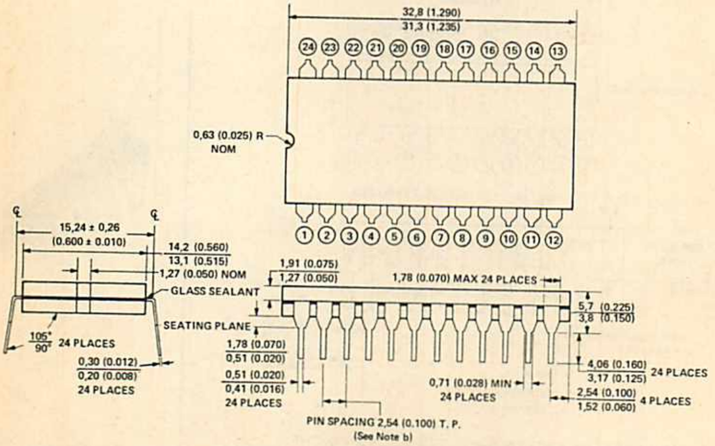


ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

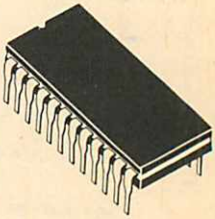
J ceramic dual-in-line packages (continued)

24-PIN JW CERAMIC



Falls within JEDEC MO-015AA dimensions

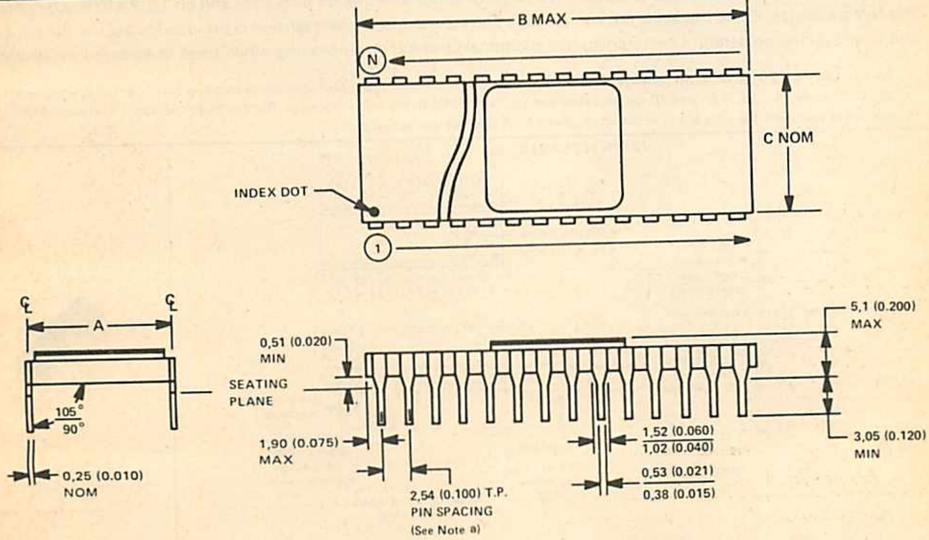
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.



NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

ceramic packages – side-braze (JD suffix)

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.



DIM \ PINS	24	28	40	48	52	64
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B MAX	31,8 (1.25)	36,8 (1.45)	52,1 (2.05)	62,2 (2.45)	67,3 (2.65)	82,6 (3.25)
C NOM	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	22,6 (0.890)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

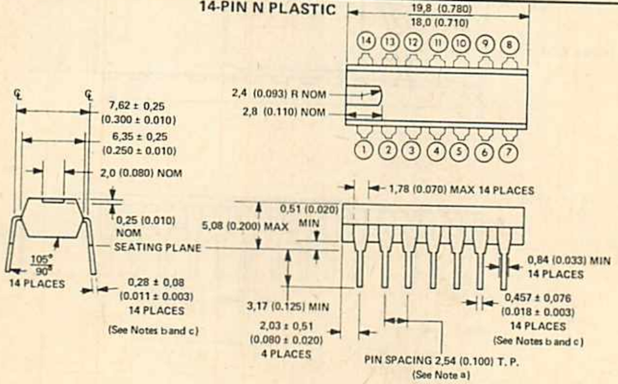
MECHANICAL DATA

N plastic packages (including NT and NW dual-in-packages)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers for the NT packages and on 15,24 (0.600) centers for the NW packages. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, 20-, and 28-pin packages, the letter N is used by itself since these packages are available in only one row-spacing width – 7,62 (0.300) for the 14-, 16-, 18-, and 20-pin packages and 15,24 (0.600) for the 28-pin package. For the 24-pin package, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.

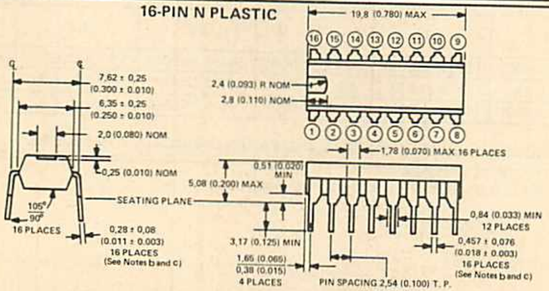
14-PIN N PLASTIC

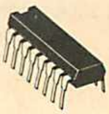


Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

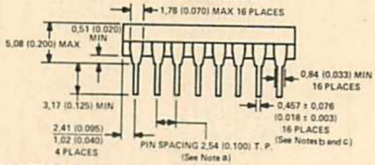
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

16-PIN N PLASTIC





ALTERNATE SIDE VIEW



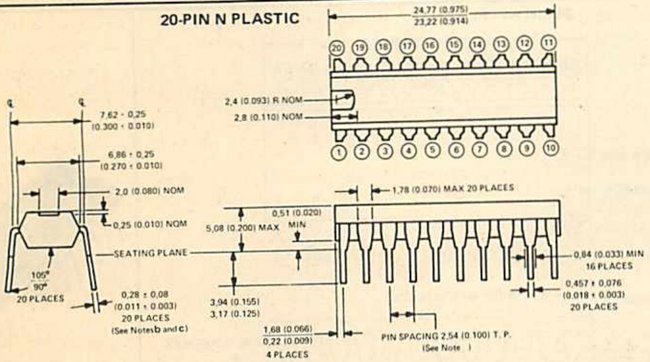
Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe. In this case, the overall length of the package is 22,1 (0.870) max.

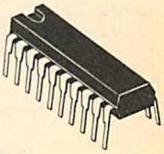
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTES:
a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
b. This dimension does not apply for solder-dipped leads.
c. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

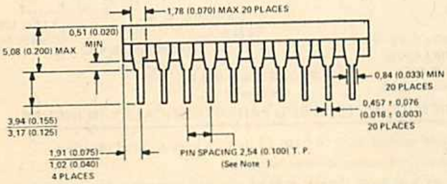
N plastic dual-in-line packages (continued)

20-PIN N PLASTIC





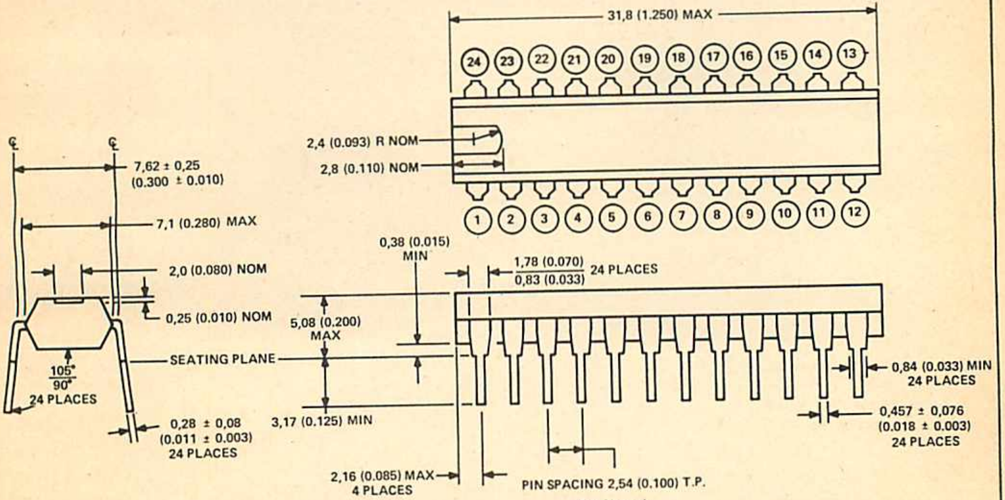
ALTERNATE SIDE VIEW


1,78 (0.070) MAX 20 PLACES
0,51 (0.020) MIN
5,08 (0.200) MAX
3,94 (0.155) / 3,17 (0.125)
0,84 (0.033) MIN 20 PLACES
0,457 ± 0,076 (0.018 ± 0.003) 20 PLACES
1,91 (0.075) / 1,02 (0.040) 4 PLACES
PIN SPACING 2,54 (0.100) T. P. (See Note)

Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe. In this case, the overall length of the package is 26,7 (1.050) max.

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

24-PIN NT PLASTIC, 0.300-INCH ROW SPACING

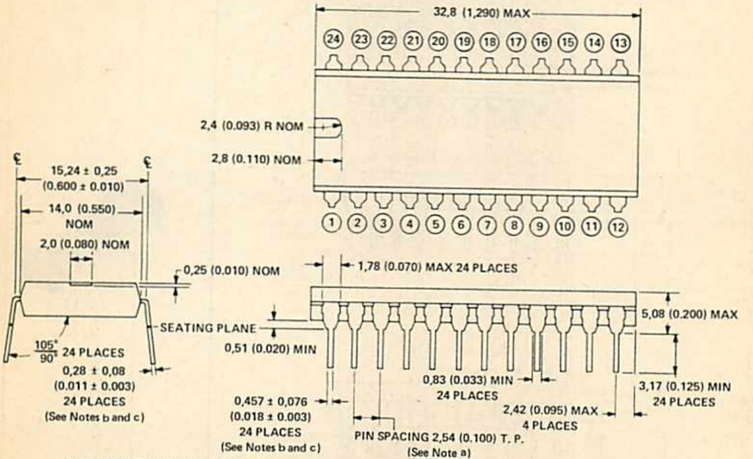


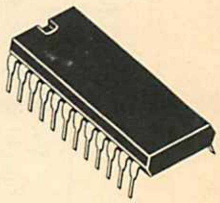
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTES:
- a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
- b. This dimension does not apply for solder-dipped leads.
- c. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line packages (continued)

24-PIN NW PLASTIC

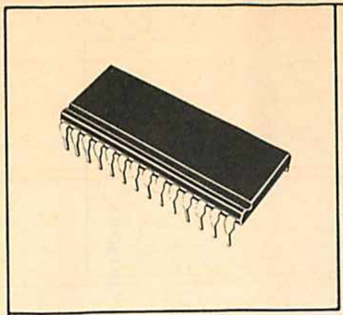




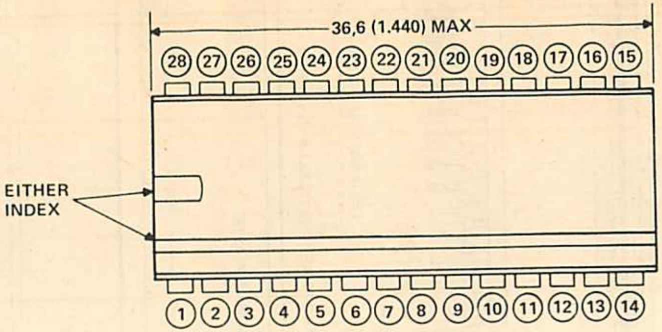
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

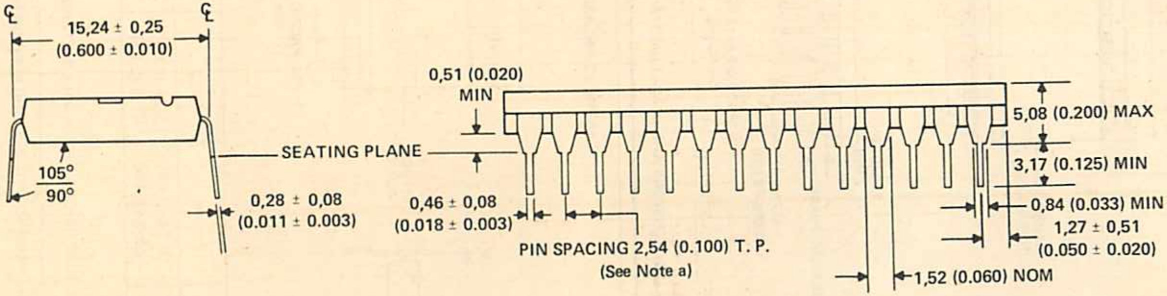
NOTES:
a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
b. This dimension does not apply for solder-dipped leads.
c. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic packages (continued)



28-PIN N PLASTIC





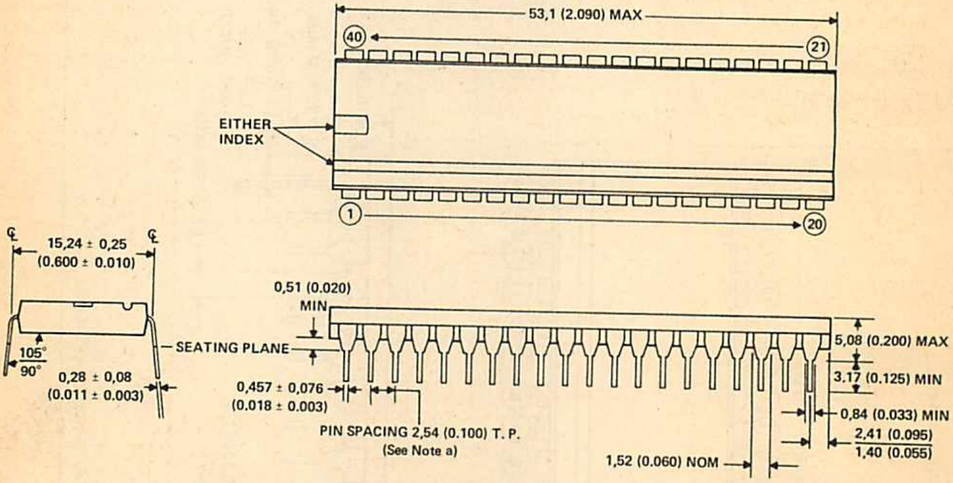
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

MECHANICAL DATA

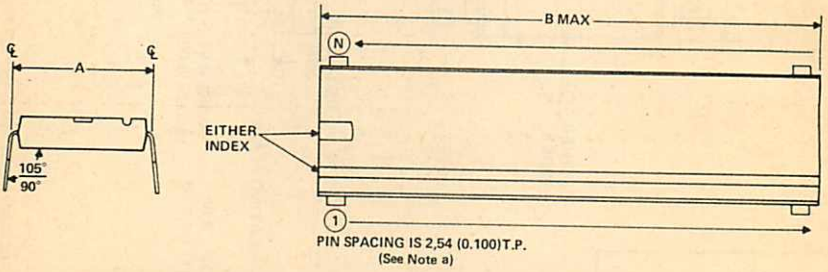
N plastic packages (continued)

40-PIN N PLASTIC



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

48-PIN, 52-PIN, AND 64-PIN N PLASTIC



DIM \ PINS	48	52	64
A ± 0,25 (0.010) B MAX	15,24 (0.600) 62,2 (2.45)	15,24 (0.600) 67,3 (2.65)	22,86 (0.900) 81,3 (3.20)

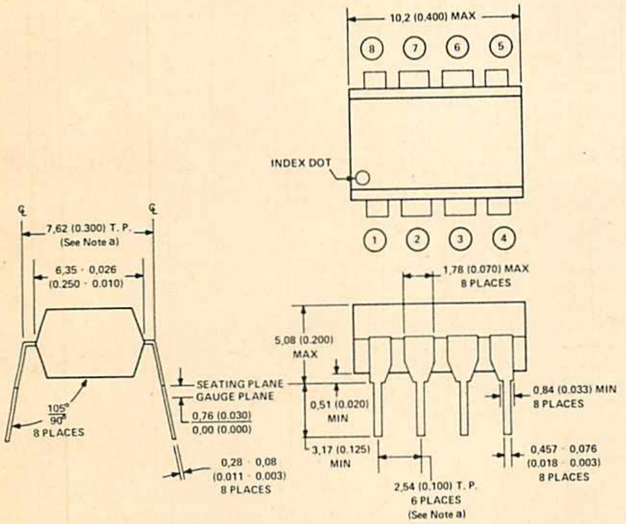
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

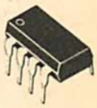
NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

P plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on an 8-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62-mm (0.300) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated leads require no additional cleaning or processing when used in soldered assembly.

8-PIN P PLASTIC





ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin is within 0,13 (0.0005) radius of true position (TP) at the gauge plane with maximum material condition and unit installed.

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TI Sales Offices

ALABAMA: Huntsville, 500 Wynn Drive, Suite 514, Huntsville, AL 35805, (205) 837-7530.

ARIZONA: Phoenix, P.O. Box 35160, 8102 N. 23rd Ave., Suite A, Phoenix, AZ 85021, (602) 995-1007.

CALIFORNIA: El Segundo, 831 S. Douglas St., El Segundo, CA 90245, (213) 973-2571; **Irvine,** 17891 Cartwright Rd., Irvine, CA 92714, (714) 660-1200; **Sacramento,** 1900 Point West Way, Suite 171, Sacramento, CA 95815, (916) 929-1521; **San Diego,** 4333 View Ridge Ave., Suite B., San Diego, CA 92123, (714) 278-9600; **Santa Clara,** 5353 Betsy Ross Dr., Santa Clara, CA 95054, (408) 980-9000; **Woodland Hills,** 21220 Erwin St., Woodland Hills, CA 91367, (213) 704-7759.

COLORADO: Denver, 9725 E. Hampden St., Suite 301, Denver, CO 80231, (303) 695-2800.

CONNECTICUT: Wallingford, 9 Barnes Industrial Park Rd., Barnes Industrial Park, Wallingford, CT 06492, (203) 269-0074.

FLORIDA: Ft. Lauderdale, 2765 N.W. 62nd St., Ft. Lauderdale, FL 33309, (305) 973-8502; **Maitland,** 2601 Maitland Center Parkway, Maitland, FL 32751, (305) 646-9600; **Tampa,** 5010 W. Kennedy Blvd., Suite 101, Tampa, FL 33609, (813) 870-6420.

GEORGIA: Atlanta, 3300 Northeast Expy., Building 9, Atlanta, GA 30341, (404) 452-4600.

ILLINOIS: Arlington Heights, 515 W. Algonquin, Arlington Heights, IL 60005, (312) 640-2934.

INDIANA: Ft. Wayne, 2020 Inwood Dr., Ft. Wayne, IN 46815, (219) 424-5174; **Indianapolis,** 2346 S. Lynhurst, Suite J-400, Indianapolis, IN 46241, (317) 248-8555.

IOWA: Cedar Rapids, 373 Collins Rd. NE, Suite 200, Cedar Rapids, IA 52402, (319) 395-9550.

MARYLAND: Baltimore, 1 Rutherford Pl., 7133 Rutherford Rd., Baltimore, MD 21207, (301) 944-8600.

MASSACHUSETTS: Waltham, 504 Totten Pond Rd., Waltham, MA 02154, (617) 895-9100.

MICHIGAN: Farmington Hills, 33737 W. 12 Mile Rd., Farmington Hills, MI 48018, (313) 553-1500.

MINNESOTA: Edina, 7625 Parklawn, Edina, MN 55435, (612) 830-1600.

MISSOURI: Kansas City, 8080 Ward Pkwy., Kansas City, MO 64114, (816) 523-2500; **St. Louis,** 11861 Westline Industrial Drive, St. Louis, MO 63141, (314) 569-7600.

NEW JERSEY: Clark, 292 Terminal Ave. West, Clark, NJ 07066, (201) 574-9800.

NEW MEXICO: Albuquerque, 5907 Alice NSE, Suite E., Albuquerque, NM 87110, (505) 265-8491.

NEW YORK: East Syracuse, 6700 Old Collamer Rd., East Syracuse, NY 13057, (315) 463-9291; **Endicott,** 112 Nanticoke Ave., P.O. Box 618, Endicott, NY 13760, (607) 754-3900; **Melville,** 1 Huntington Quadrangle, Suite 3C10, P.O. Box 2936, Melville, NY 11747, (516) 454-6600; **Poughkeepsie,** 385 South Rd., Poughkeepsie, NY 12601, (914) 473-2900; **Rochester,** 1210 Jefferson Rd., Rochester, NY 14623, (716) 424-5400.

NORTH CAROLINA: Charlotte, 8 Woodlawn Green, Woodlawn Rd., Charlotte, NC 28210, (704) 527-0930; **Raleigh,** 2809 Highwoods Blvd., Suite 100, Raleigh, NC 27625, (919) 876-2725.

OHIO: Beachwood, 23408 Commerce Park Rd., Beachwood, OH 44122, (216) 464-6100; **Dayton,** Kingsley Bldg., 4124 Linden Ave., Dayton, OH 45432, (513) 258-3877.

OKLAHOMA: Tulsa, 7615 East 63rd Place, 3 Memorial Place, Tulsa, OK 74133, (918) 250-0633.

OREGON: Beaverton, 6700 SW 105th St., Suite 110, Beaverton, OR 97005, (503) 643-6758.

PENNSYLVANIA: Ft. Washington, 260 New York Dr., Ft. Washington, PA 19034, (215) 643-6450; **Coraopolis,** 420 Rouser Rd., 3 Airport Office Park, Coraopolis, PA 15108, (412) 771-8550.

TEXAS: Austin, 12501 Research Blvd., P.O. Box 2909, Austin, TX 78723, (512) 250-7655; **Dallas,** 1001 E. Campbell Rd., Richardson, TX 75080, (214) 680-5082; **Houston,** 9100 Southwest Frwy., Suite 237, Houston, TX 77036, (713) 778-6592; **San Antonio,** 1000 Central Parkway South, San Antonio, TX 78232, (512) 496-1779.

UTAH: Murray, 5201 South Green SE, Suite 200, Murray, UT 84107, (801) 266-8972.

VIRGINIA: Fairfax, 3001 Prosperity, Fairfax, VA 22031, (703) 849-1400.

WISCONSIN: Brookfield, 450 N. Sunny Slope, Suite 150, Brookfield, WI 53005, (414) 785-7140.

WASHINGTON: Redmond, 2723 152nd Ave., N.E. Bldg. 6, Redmond, WA 98052, (206) 881-3080.

CANADA: Ottawa, 436 McLaren St., Ottawa, Ontario, Canada, K2P0M8,(613) 233-1177; **Richmond Hill,** 280 Centre St. E., Richmond Hill L4C1B1, Ontario, Canada, (416) 884-9181; **St. Laurent,** Ville St. Laurent Quebec, 9460 Trans Canada Hwy., St. Laurent, Quebec, Canada H4S1R7, (514) 334-3635.

E

TI Regional Technology Centers

CALIFORNIA: Northern, 5353 Betsy Ross Dr., Santa Clara, CA 95054, (408) 748-2220, Hotline: (408) 980-0305. **Southern,** 17891 Cartwright Rd., Irvine, CA 92714, (714) 660-8140, Hotline: (714) 660-8164.

GEORGIA: Atlanta, 3300 Northeast Expressway, Building 8, Atlanta, GA 30341, (404) 452-4682, Hotline: (404) 452-4686.

ILLINOIS: Chicago, 515 W. Algonquin Road, Arlington Heights, IL 60005, (312) 640-2909, Hotline: (312) 228-6008.

MASSACHUSETTS: Boston, 400-2 Totten Pond Road, Waltham, MA 02154, (617) 890-6671, Hotline: (617) 890-4271.

TEXAS: Dallas, 1001 E. Campbell Rd., Richardson, TX 75081, (214) 680-5066, Hotline: (214) 680-5096.

TI Distributors

ALABAMA: Arrow (205) 882-2730; Marshall (205) 881-9235.

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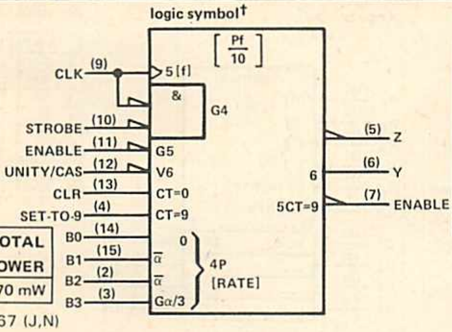
BE

167

SYNCHRONOUS DECADE RATE MULTIPLIERS

logic symbol†



typical performance

TYPE	COUNT FREQ	CLEAR	TOTAL POWER
'167	25 MHz	ASYNC-H	270 mW

SN54167 (J,FH) SN74167 (J,N)

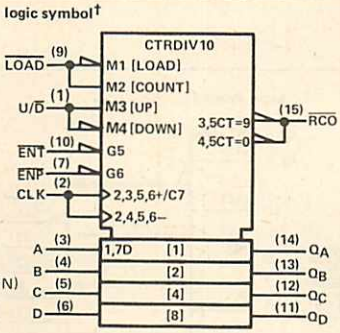
pin assignments

J, N PACKAGES				FH PACKAGE			
1	nc	9	CLK	1	nc	11	nc
2	B2	10	STRB	2	nc	12	CLK
3	B3	11	ENin	3	B2	13	STRB
4	SET-TO-9	12	UNITY/CAS	4	B3	14	ENin
5	Z	13	CLR	5	SET-TO-9	15	UNITY/CAS
6	Y	14	B0	6	nc	16	nc
7	ENout	15	B1	7	Z	17	CLR
8	GND	16	V_{CC}	8	Y	18	B0
				9	ENout	19	B1
				10	GND	20	V_{CC}

168

4-BIT UP/DOWN SYNCHRONOUS COUNTERS (decade)

logic symbol†



typical performance

TYPE	COUNT FREQ	TOTAL POWER
'ALS168A	40 MHz	75 mW
'AS168		
'S168	40 MHz	500 mW

SN54ALS168A (J,FH) SN74ALS168A (N,FN)
SN54AS168 (J,FH) SN74AS168 (N,FN)
SN54S168 (J,FH) SN74S168 (J,N,FN)

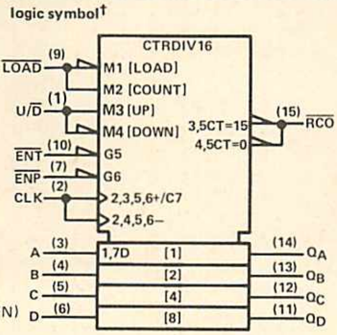
pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	U/$\overline{\text{D}}$	9	$\overline{\text{LOAD}}$	1	nc	11	nc
2	CLK	10	$\overline{\text{ENT}}$	2	U/$\overline{\text{D}}$	12	$\overline{\text{LOAD}}$
3	A	11	Q_D	3	CLK	13	$\overline{\text{ENT}}$
4	B	12	Q_C	4	A	14	Q_D
5	C	13	Q_B	5	B	15	Q_C
6	D	14	Q_A	6	nc	16	nc
7	$\overline{\text{ENP}}$	15	$\overline{\text{RCO}}$	7	C	17	Q_B
8	GND	16	V_{CC}	8	D	18	Q_A
				9	$\overline{\text{ENP}}$	19	$\overline{\text{RCO}}$
				10	GND	20	V_{CC}

169

4-BIT UP/DOWN SYNCHRONOUS COUNTERS (binary)

logic symbol†



typical performance

TYPE	COUNT FREQ	TOTAL POWER
'ALS169A	40 MHz	75 mW
'AS169		
'LS169B	35 MHz	140 mW
'S169	40 MHz	500 mW

SN54ALS169A (J,FH) SN74ALS169A (N,FN)
SN54AS169 (J,FH) SN74AS169 (N,FN)
SN54LS169B (J,FH) SN74LS169B (J,N,FN)
SN54S169 (J,FH) SN74S169 (J,N,FN)

pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	U/$\overline{\text{D}}$	9	$\overline{\text{LOAD}}$	1	nc	11	nc
2	CLK	10	$\overline{\text{ENT}}$	2	U/$\overline{\text{D}}$	12	$\overline{\text{LOAD}}$
3	A	11	Q_D	3	CLK	13	$\overline{\text{ENT}}$
4	B	12	Q_C	4	A	14	Q_D
5	C	13	Q_B	5	B	15	Q_C
6	D	14	Q_A	6	nc	16	nc
7	$\overline{\text{ENP}}$	15	$\overline{\text{RCO}}$	7	C	17	Q_B
8	GND	16	V_{CC}	8	D	18	Q_A
				9	$\overline{\text{ENP}}$	19	$\overline{\text{RCO}}$
				10	GND	20	V_{CC}

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† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

170

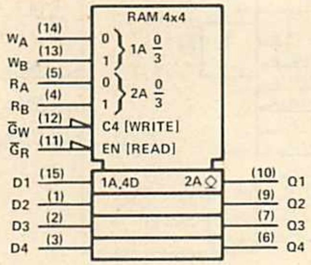
4-BY-4 REGISTER FILES

typical performance

TYPE	TYPE OF OUTPUT	ADDRESS TIME	POWER PER BIT
'170	O-C	30 ns	40 mW
'LS170	O-C	27 ns	7.8 mW

SN54170 (J,FH) SN74170 (J,N)
SN54LS170 (J,FH) SN74LS170 (J,N,FN)

logic symbol[†]



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	D2	9	Q2	1	nc	11	nc
2	D3	10	Q1	2	D2	12	Q2
3	D4	11	$\overline{G}_R$	3	D3	13	Q1
4	R_B	12	$\overline{G}_W$	4	D4	14	$\overline{G}_R$
5	R_A	13	W_B	5	R_B	15	$\overline{G}_W$
6	Q4	14	W_A	6	nc	16	nc
7	Q3	15	D1	7	R_A	17	W_B
8	GND	16	V_{CC}	8	Q4	18	W_A
				9	Q3	19	D1
				10	GND	20	V_{CC}

171

QUAD D-TYPE FLIP-FLOPS WITH CLEAR

- Double-Rail Outputs
- Buffered Clock and Clear Inputs
- Individual Data Inputs to Each Flip-Flop

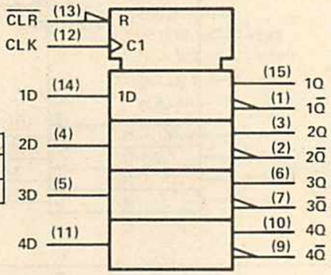
typical performance

TYPE	FREQ	POWER PER F-F	DELAY TIMES	
			SETUP	HOLD
'LS171	30 MHz	17.5 mW	20 ns↑	5 ns↑

↑ Rising edge of clock pulse

SN54LS171 (J,FH) SN74LS171 (J,N,FN)

logic symbol[†]



pin assignments

J, N PACKAGES				FH, FN PACKAGES			
1	$1\overline{Q}$	9	$4\overline{Q}$	1	nc	11	nc
2	$2\overline{Q}$	10	4Q	2	$1\overline{Q}$	12	$4\overline{Q}$
3	2Q	11	4D	3	$2\overline{Q}$	13	4Q
4	2D	12	CLK	4	2Q	14	4D
5	3D	13	$\overline{CLR}$	5	2D	15	CLK
6	3Q	14	1D	6	nc	16	nc
7	$3\overline{Q}$	15	1Q	7	3D	17	$\overline{CLR}$
8	GND	16	V_{CC}	8	3Q	18	1D
				9	$3\overline{Q}$	19	1Q
				10	GND	20	V_{CC}

For chip carrier information, contact the factory.

[†] Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

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